DESIGN AND PERFORMANCE OF A MULTIPLE-LOOP FREQUENCY SYNTHESIZER

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THESIS

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ABSTRACT

This report presents the results of the design and fabrication of a Multiple-Loop Frequency Synthesizer. The design utilizes frequency control loops to extend the capture range of a phase-locked loop used to provide frequency stability. No harmonic generators, mixers or filters are used, in the usual sense; a single crystal oscillator is required. The synthesizer is small, light weight, accurate to within $\pm$ 0.0025% of the programmed frequency, covers the AM broadcast band (500 kHz to 1600 kHz), and is electronically tunable in 10 kHz steps. Unwanted sidebands 5 kHz and 10 kHz away from the programmed frequency have relative magnitudes of -28 db and -40 db, respectively.

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I. INTRODUCTION

A. BACKGROUND AND DEFINITIONS

In the past, inductance-capacitance (LC) oscillators or crystal oscillators were used to generate fixed-frequency sine waves. These signal generators are used as (1) local oscillators in receivers, (2) frequency sources in transmitters, and (3) as oscillators for instrumentation purposes.

LC oscillators provide broad frequency coverage with relative ease of frequency selection; however, the frequency stability of these oscillators is not adequate for many applications such as non-synchronous communications systems, and transmitters and receivers where rapid, accurate frequency acquisition is necessary.

Frequency stability is defined as the ability of an oscillator to maintain a desired frequency. Stability is expressed as per cent deviation from the assigned frequency value. [Ref. 1] Frequency stability for transmitters, for example, may vary from 0.003% to 0.1% of the assigned frequency. [Ref. 2] Sources having better stability are often required to maintain precise synchronization in modern electronic systems, such as high speed digital computers, digital data systems and control systems.

Frequency stability can be improved by using a crystal oscillator, but the range of frequencies available from one oscillator is limited to a small band about the resonant frequency of the oscillator or to harmonics of the crystal frequency. Discrete frequency selection is possible when using a crystal oscillator by changing the crystal in the oscillator circuit or by using harmonics of the crystal frequency.

Various methods are used to combine the best features of both the LC oscillator and the crystal oscillator. One such method is to synchronize an LC oscillator with the crystal oscillator. In this configuration, the LC oscillator is used as a frequency-selective filter. The LC oscillator is tuned to either the fundamental frequency of the crystal oscillator or to one of its harmonics. If the crystal oscillator output is rich in harmonics, it is possible to obtain a wide range of discrete frequencies.

However, the requirement remains for an oscillator with crystal oscillator frequency stability and LC oscillator frequency selection capability. Oscillators having this capability are referred to as frequency synthesizers. A frequency synthesizer is an instrument which translates the frequency stability of a single frequency to any one of many other possible frequencies usually over a broad spectrum. Its single-frequency generator is usually of frequency standard quality; thus, the synthesizer may be called a frequency standard capable of furnishing a large number of frequencies. [Ref. 3]

B. SYNTHESIZER DESIGN PHILOSOPHIES

There are two basic approaches to frequency synthesis known as "direct" and "indirect". Direct synthesis performs a series of arithmetic operations (multiplication, division, addition, subtraction) on the signal from the frequency standard to achieve an output signal having the desired frequency. The indirect method uses tunable oscillators, which are phase-locked to harmonics of a standard frequency. [Ref. 3] If, for example, the desired frequency is 4326 kHz, then there are two extreme possibilities in design, namely:

(1) take the sum of the 4th harmonic of 1000 kHz, the 3rd harmonic of 100 kHz, the 2nd harmonic of 10 kHz, and the 6th harmonic of 1.0 kHz, or

(2) take the 4326th harmonic of 1.0 kHz.

Various combinations of (1) and (2) are possible. The fundamental techniques to be applied are thus the generation of harmonics (multiplication) and addition of harmonics. The state-of-the-art in the field of harmonic generators makes possible the generation of a large number of harmonics, thereby reducing the number of summations and the number of reference frequencies required. The main difficulty in the second method is that very pure harmonics are desired, and therefore good filtering of unwanted components is necessary.

Two methods of performing the multiplication and addition of frequencies are:

(1) the passive or frequency-synthesis method using only harmonic generators, mixers, and filters;

(2) the loop systems method in which the frequency of an oscillator is compared with the frequency to be multiplied or added; this is called frequency analysis.

The advent of digital frequency division techniques allows frequency division by any whole number N. This division capability further reduces the number of addition operations and reference frequencies required. Sophisticated synthesizer systems may use a combination of these methods. Present synthesizer designs favor the loop systems method. Additional information on these methods can be found in Reference 4.

As mentioned previously, stability is one of the most important attributes of frequency synthesizers. If the frequency stability of the

output signal is to be maintained at the same level as that of the stable source (frequency standard), then the frequency selected must be derived from the stable source. Other factors to be considered in the design of a frequency synthesizer are: (1) purity of the generated signal — the absence of unwanted sidebands, noise and intermodulation (spurious) components (2) tuning (3) size (4) frequency band covered (5) frequency step size and (6) power required.

The design considered in this report differs from that of early frequency synthesizers in that no harmonic generators, frequency mixers, or filters are used, in the usual sense; Programmable dividers are used to generate the desired frequency. A unique feature of the frequency synthesizer reported on here is the use of two additional control loops (coarse and fine) to extend the operating range of the synthesizer beyond the capture range of the phase-locked loop used to maintain a stable output. The fine and coarse loops use integrated circuit (IC) pulse-counting discriminators as frequency-to-voltage transducers. Except for the crystal oscillator and thumbwheel switches used to select the desired frequency, this frequency synthesizer is constructed of IC's including the phase-locked loop (PLL). In the remainder of this report, we refer to the device designed, built and tested as a part of this research as the multiple-loop frequency synthesizer (MLFS).

C. MULTIPLE-LOOP FREQUENCY SYNTHESIZER

The MLFS design considered in this report is somewhat different from previous designs in that the MLFS technique utilizes frequency-control loops containing frequency discriminators. Frequency discriminators do not normally possess the frequency stability required for use in a synthesizer.

In the design of the MLFS, a free-running voltage-controlled multivibrator, hereafter referred to as the VCO, is used as the primary oscillator. A subharmonic of the VCO output signal is compared with the output of a crystal oscillator (stable reference source) by means of a phase comparator. The VCO is locked in phase with the reference source through its Nth subharmonic. This provides frequency stability comparable to the frequency stability of the reference source. The Nth subharmonic is obtained by dividing the VCO output frequency with a digital decade counter circuit. The VCO output frequency f_o is given by the equation $f_o = (N \times f_r)$ where f_r is the frequency of the reference source. Fig. 1 is a simplified block diagram of the MLFS. The VCO and phase comparator are integral parts of the PLL.

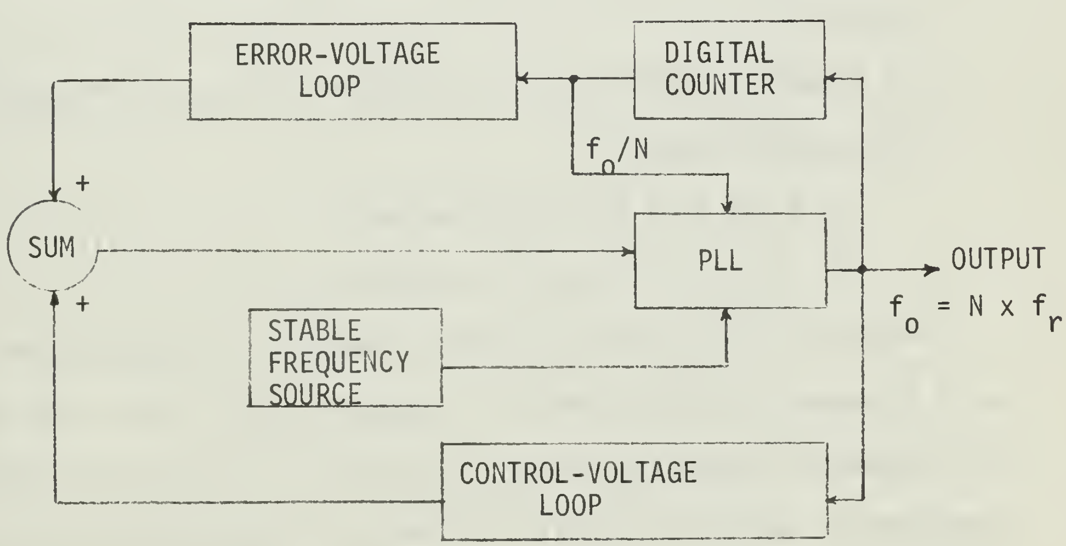


Fig. 1. BLOCK DIAGRAM OF THE MLFS SHOWING THE CONTROL LOOPS

The design of the MLFS utilizes three control loops. They are the

(1) control voltage loop used for coarse tuning;

(2) error voltage loop which generates an error voltage used to change frequencies and to correct for large frequency discrepancies;

(3) phase comparator loop used for fine tuning.

The MLFS utilizes a three pole, Binary Coded Decimal (BCD) switch to program the digital counter for electronic tuning. This synthesizer is readily adaptable to microminiaturization by using large scale integration (LSI) fabrication techniques.

D. RESULTS OF THIS RESEARCH

A MLFS having the following characteristics was designed, built and tested.

(1) tuning range: 0.5 MHz to 1.6 MHz (AM broadcast band);

(2) electronic tunable in 10 kHz steps (separation of AM broadcast stations);

(3) frequency stability of ± 0.0025% of the output frequency.

(4) spurious output

(a) 5 kHz side band 28 db below f_o

(b) 10 kHz side band 40 db below f_o

Results of this research clearly show that frequency-control loops, with frequency discriminators, in conjunction with a PLL, can be used in frequency synthesizers and still maintain frequency stability. Furthermore, multiple crystal oscillators, harmonic generators, mixers, and filters are not required in synthesizers using one or more control loops.

E. REPORT CONTENTS

Chapter II of this report lists the important performance characteristics of the MLFS. System design of the MLFS is presented in Chapter III. Chapter IV deals with subsystem design and system alignment. Chapter V lists conclusions and recommendations. Appendix A gives the detailed design of each stage in the system. A list of references is provided.

II. SUMMARY OF PERFORMANCE CHARACTERISTICS

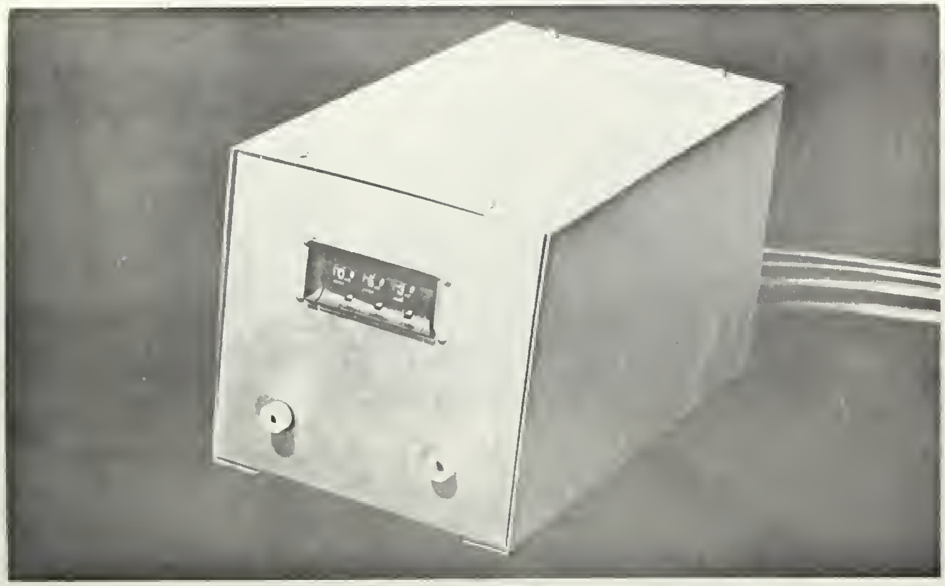
Photographs of the MLFS built during the course of this study are shown in Figs. 2. Fig. 2b indicates the compartmentation used to reduce radio-frequency interference. The relatively large unused compartment was to contain the power supply and the rest of the circuitry of an AM receiver.

The performance characteristics of the MLFS are summarized in Table I.

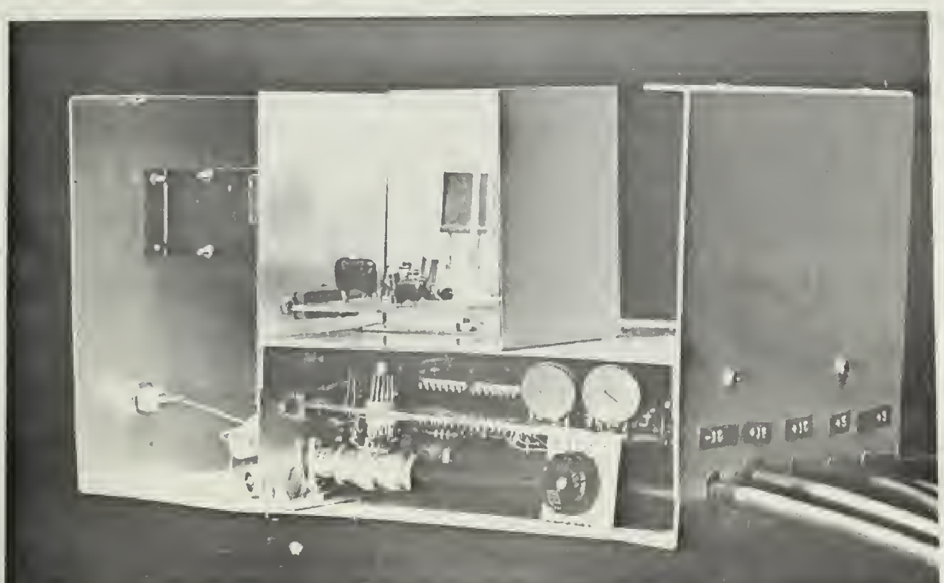
Frequency accuracy was determined using a CP-814/USM-207 electronic counter and a Monsanto counter-timer model 100B. The output frequency was monitored for one week for each counter. Readings were taken at random. The observed accuracy of ±10 Hz is less than ±0.0025% at 500 kHz; however, ±0.0025% is the guaranteed accuracy of the reference crystal oscillator. The accuracy of the synthesizer is determined then by the accuracy of the reference crystal oscillator.

Slew rate is the rate of frequency change. The slew rate was determined by observing the output of a Hewlett Packard model 5210A frequency meter (discriminator). Fig. 3a is the frequency discriminator output for an increase in frequency of 1.0 MHz, and Fig. 3b is the output for a decrease in frequency of 1.0 MHz. The slew rate is greater for a decrease in frequency because the VCO is being driven toward its preferred (free-running) frequency.

Spurious outputs were measured using a Hewlett Packard Spectrum Analyzer model 141A with plug-in units 8553L RF section, 8552A IF section, and 141S display section. Photographs of the output spectrum



(a) FRONT VIEW OF MLFS. The synthesizer is programmed with the rotary thumbwheel switch mounted on the front of the synthesizer.



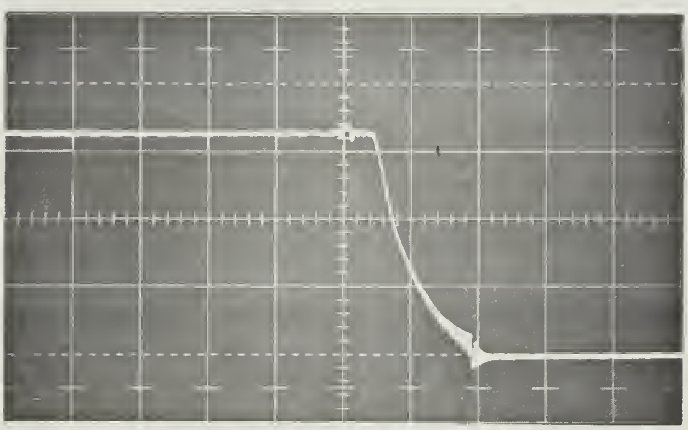
(b) REAR VIEW OF MLFS. The reference crystal oscillator is in the upper compartment. The balance of the synthesizer is in the lower compartment. The cables provide power to the units.

Fig. 2. Photographs of the Multiple-Loop Frequency Synthesizer

TABLE I. CHARACTERISTICS OF THE MLFS

Characteristic	Remarks
1. Frequency Range: 500 kHz to 1600 kHz	1. Tunable in 10 kHz steps.
2. Frequency Selection: electronically tuned	2. The synthesizer is electronically tuned by selecting the frequency and programming the digital decade counter with three Binary Coded Decimal thumbwheel switches.
3. Output Waveform: square wave	3. Output voltage $\geq$ 3 volts peak-to-peak (see Fig. 5).
4. Frequency Stability: $\pm 0.0025\%$	4. The maximum frequency deviation observed is ± 10 Hz. See page 15.
5. Slew Rates: 6.9 MHz/sec for an increase in frequency and 11.1 MHz/sec for a decrease in frequency	5. These slew rates were calculated using Fig. 3. See page 15.
6. Power Requirements: +18V at 35 ma +10V at 45 ma + 5V at 300 ma + 3V at 10 ma -10V at 40 ma	
7. Spurious Level: 5 kHz at -28 db 10 kHz at -40 db	7. See page 15.
8. Stability of Components and Circuit:	8. No tests were conducted.

a. Discriminator output for an increase in frequency from 500 kHz to 1500 kHz.



b. Discriminator output for a decrease in frequency from 1500 kHz to 500 kHz.

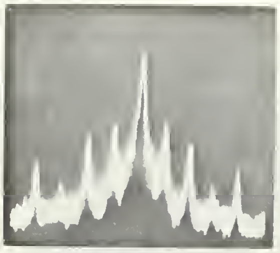
Fig. 3. PHOTOGRAPHS OF THE MLFS RESPONSE TO A STEP CHANGE IN FREQUENCY FROM 500 kHz TO 1500 kHz. The vertical and horizontal scales are 2 volts/cm and 50 msec/cm respectively.

for f_0 = 500 kHz are shown in Fig. 4. Fig. 4a was taken using the Hewlett Packard Analyzer in the log mode. The dispersion is 5 kHz/div. Comparing the side bands to the center frequency, 5 kHz is -28 db and 10 kHz is -40 db. Figures 4b and 4c were taken using a Tektronix oscilloscope model 3L5 with spectrum analyzer plug-in. The vertical scale in both pictures is uncalibrated.

Sample synthesizer-output waveforms are shown in Fig. 5. Fig. 6 shows the output of the Hewlett Packard frequency discriminator for discrete frequency changes of 100 kHz and 10 kHz. Fig. 7 is the output waveform of the 2 MHz reference crystal oscillator. When properly aligned the performance of the MLFS is very good. The output frequency is as programmed with no false lock up during switching of frequency. Alignment procedure is straightforward and is presented in Chapter IV.

The MLFS step size can be 10 kHz, 100 kHz, or 1 MHz, or combinations of these steps provided the end frequency is within its frequency spectrum (0.5 MHz to 1.6 MHz). The only external controls on the MLFS are the three thumbwheel switches for frequency selection. These switches have the capability of providing background lights so the synthesizer can be used in total darkness. The frequency selection is a one step operation with no fine tuning or zero adjust necessary.

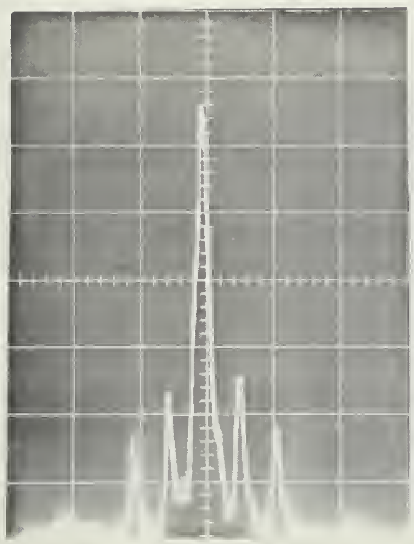
The MLFS utilizes 18 IC's and the crystal oscillator printed-circuit board. The IC count can be reduced to 12 at the present time and these could be combined into 3 or 4 IC's using large-scale-integration (LSI) fabrication techniques.



Dispersion: 5 kHz/div.
LOG Scale

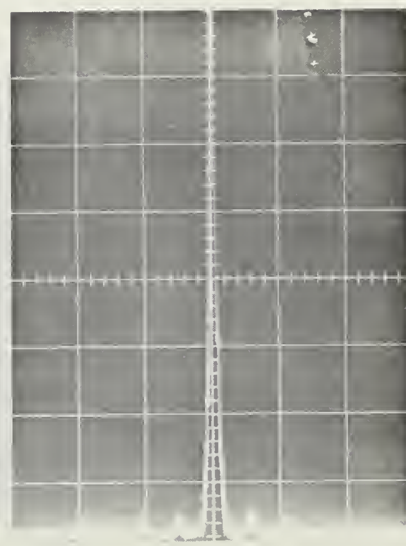
f_o

(a)



(b)

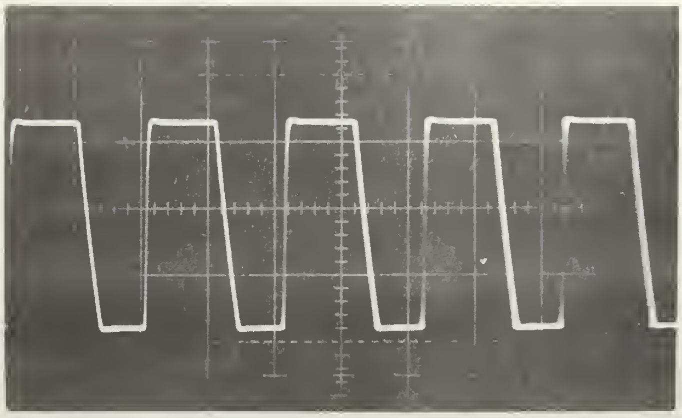
Dispersion: 10 kHz/cm
Vert: uncalibrated
LOG Scale



(c)

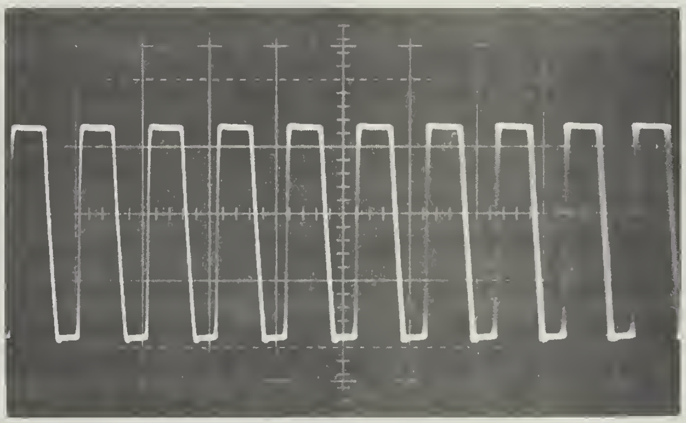
Dispersion: 10 kHz/cm
Vert: uncalibrated
Linear Scale

Fig. 4. PHOTOGRAPHS OF THE SPECTRUM OF THE MLFS OUTPUT VOLTAGE WHEN f_o = 500 kHz. (a) taken from Hewlett Packard Spectrum Analyzer (b) and (c) taken from Tektronix oscilloscope with Spectrum Analyzer unit 3L5.



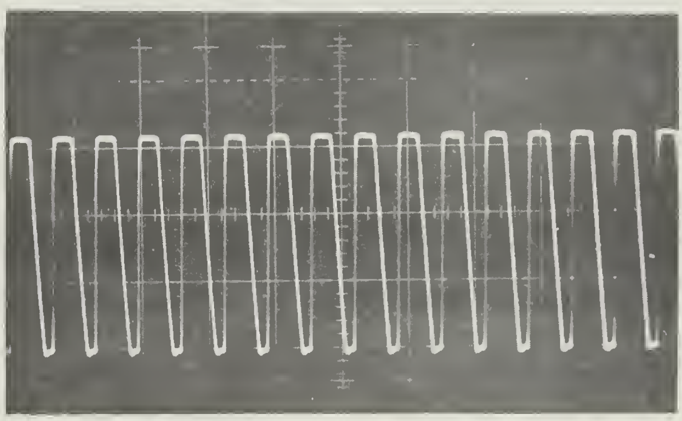
Frequency = 500 kHz

(a)



Frequency = 1.0 MHz

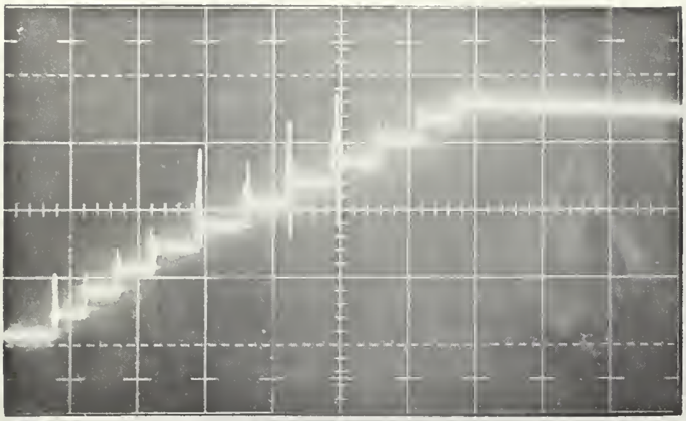
(b)



Frequency = 1.6 MHz

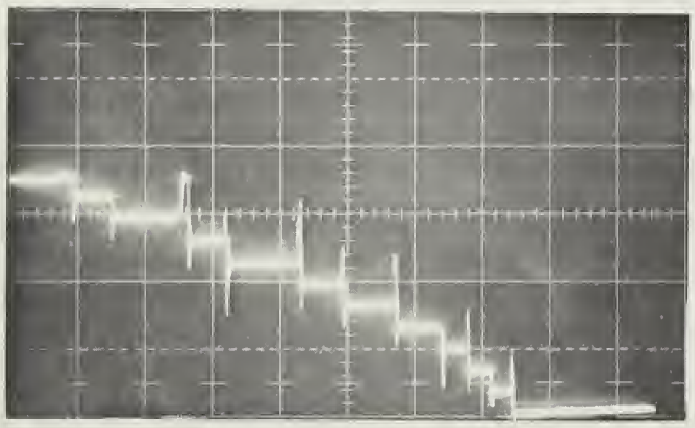
(c)

Fig. 5. PHOTOGRAPHS OF THE MLFS OUTPUT VOLTAGE
Vert. = 1.0 v/cm; Horiz. = 1.0 μsec/cm.



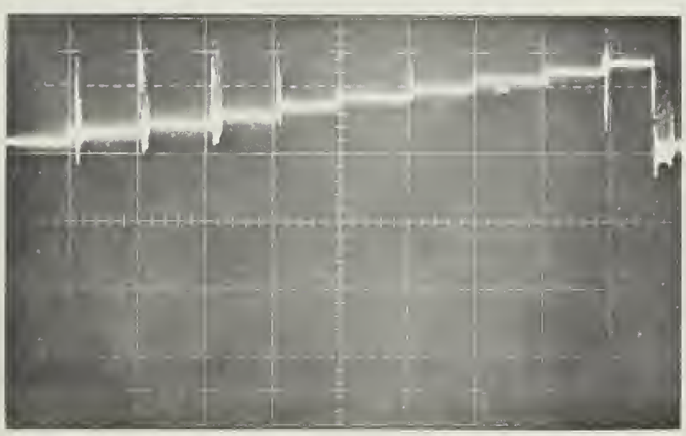
Vert. = 2.0 v/cm
Horiz. = 1.0 sec/cm
Step Size = 100 kHz
Frequency Range = 500-1500 kHz

(a)



Vert. = 2.0 v/cm
Horiz. = 1.0 sec/cm
Step Size = 100 kHz
Frequency Range = 1500-500 kHz

(b)



Vert. = 0.5 v/cm
Horiz. = 1.0 sec/cm
Step Size = 10 kHz
Frequency Range = 500-509 kHz

(c)

Fig. 6. PHOTOGRAPHS OF THE MLFS RESPONSE TO STEP CHANGES IN FREQUENCY OF 10 kHz AND 100 kHz

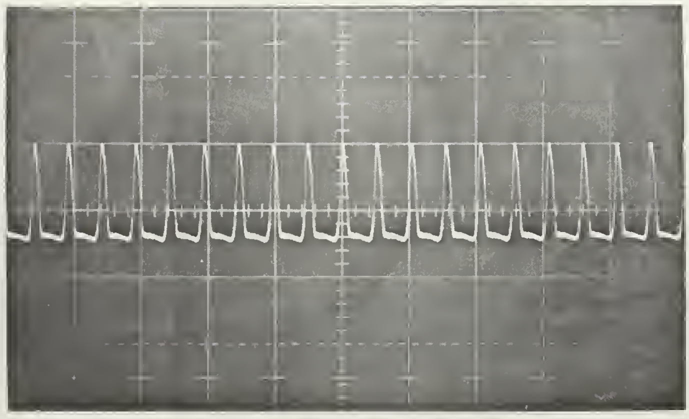


Fig. 7. PHOTOGRAPH OF THE OUTPUT VOLTAGE OF THE 2 MHz CRYSTAL OSCILLATOR.

Vert.: 1 volt/cm; Horiz.: 1.0 μsec/cm.

III. SYSTEM DESIGN

A. INITIAL CONCEPT FORMULATION

Precise tuning of a receiver, transmitter or a signal generator usually requires frequency comparison with a frequency standard and then subsequent adjustment. Use of frequency synthesizers usually makes this procedure unnecessary because of their inherent frequency stability. However, the techniques used in many synthesizers requires a large number of filters, mixers, and complicated control circuits. A result is a large and heavy piece of equipment.

The goal of this research was to design and build a frequency synthesizer that was small and light in weight and yet have most of the properties of other synthesizers. The decision was made to design and build a synthesizer that could be used to tune an AM radio to show the feasibility and application of such a synthesizer.

For the application chosen, the synthesizer must be tunable from 500 kHz to 1600 kHz in 10 kHz steps. The frequency stability, to be a synthesizer, must be as good as the reference oscillator used. Electrical tuning must be used if the physical size is to be small.

B. PRELIMINARY CONSIDERATIONS

If multiple crystals and mixers are not used in a frequency synthesizer, then some means of electrically tuning an oscillator is required. There are two general means of electrically varying the frequency of an oscillator in a continuous manner: (1) change one or more of the reactive component values (variable reactance devices — varactors) or

(2) change the conductance of the active components. The latter method was chosen for this design which means use of voltage-variable multivibrators as a voltage-controlled oscillator (VCO). In the preliminary design of a frequency synthesizer using a VCO, the following questions arise.

1. Can the necessary VCO control voltage be generated automatically?
2. Can the frequency be continuously changed in a controlled fashion?
3. Can a high degree of frequency stability be obtained using a VCO?

A voltage proportional to frequency is obtained by using the output of a frequency discriminator (demodulator), however, the transfer characteristics of the VCO and the frequency discriminator generally do not "match". The match must be quite close over the frequency region of interest. If both characteristics are linear, a match can be achieved by manipulating the output of the frequency discriminator with a corrective circuit which uses DC operational amplifiers and sum and difference circuits. A simplified block diagram of a circuit to perform this task is shown in Fig. 8a.

A method of changing the VCO frequency is to introduce a controlled error voltage into the control voltage loop. The frequency step size of the synthesizer is 10 kHz or an integer multiple of 10 kHz between 500 kHz and 1600 kHz. The common denominator of all desired frequencies is 10 kHz. By sampling the VCO output frequency or dividing the VCO output by some number N such that the output frequency of the divide-by-N circuit is 10 kHz we arrive at the common denominator. Comparing this frequency with a reference proportional to 10 kHz will give the needed

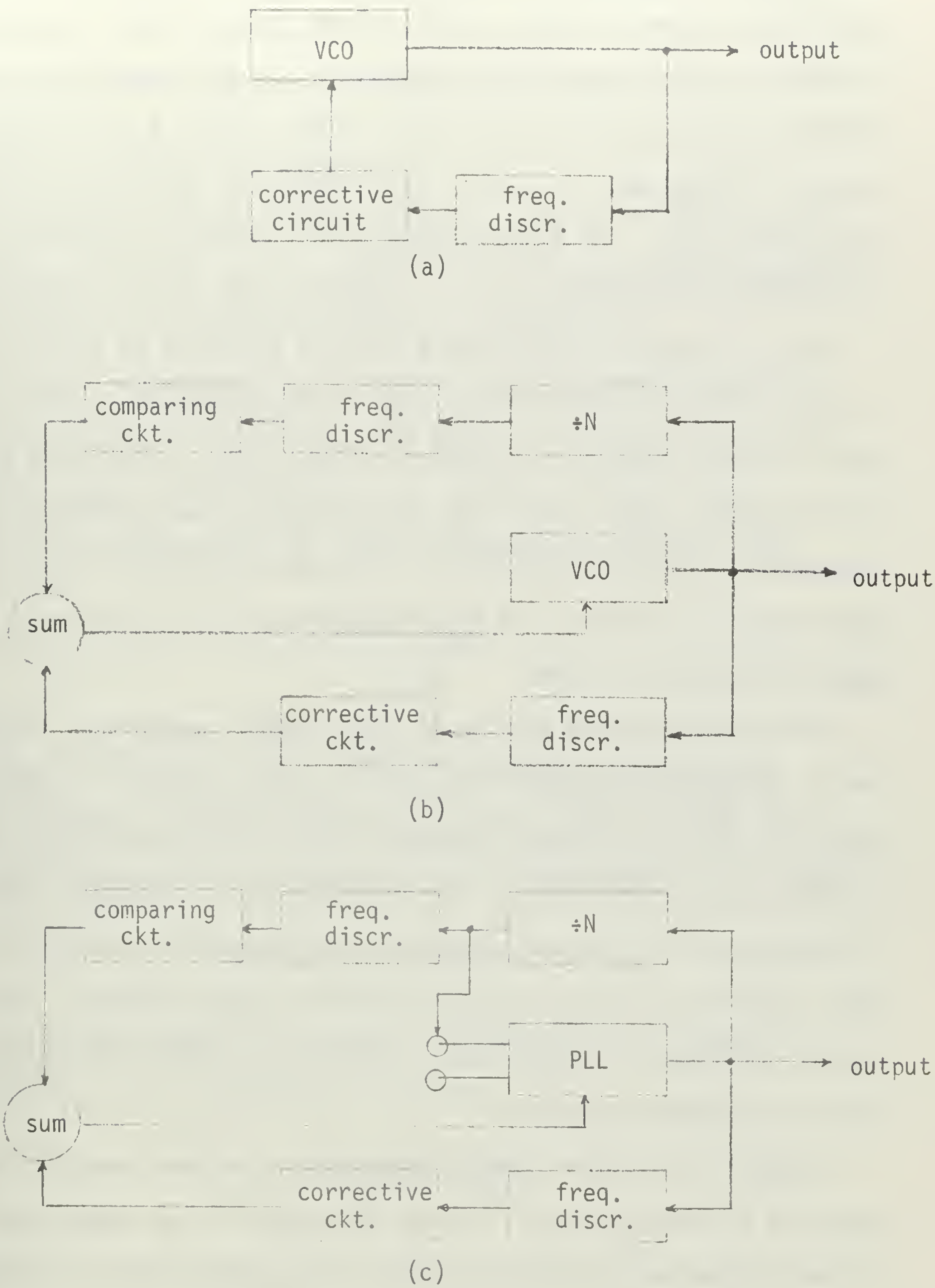


Fig. 8. EVOLUTION OF THE MLFS BLOCK DIAGRAM

error signal. A frequency discriminator provides a DC voltage proportional to the frequency f_o/N of the applied signal. Comparison of the DC voltage proportional to 10 kHz with a DC voltage of the same amplitude gives zero error for $f_o/N = 10$ kHz. When $f_o/N \neq 10$ kHz the error voltage must be of the right polarity to drive the VCO frequency back to f_o. The block diagram in Fig. 8a can be modified to incorporate an error-voltage loop. Fig. 8b is the revised block diagram.

The last question above cites a criteria difficult to satisfy using a standard VCO. To use the error loop for fine frequency control the error loop gain must be of the order of 100 to 1000. With gains of this magnitude, noise in the loop itself degrades the system and the loop becomes unstable. Reducing the loop gain to maintain stability renders the loop sluggish and unable to control the VCO output to the degree of precision desired.

The VCO was replaced with an IC phase-locked loop (PLL). The PLL used is the NE562 described in Appendix A of this report. In this particular PLL, the frequency feedback loop is available for application of externally derived signals. This permits use of the phase comparator in the PLL for fine frequency control. The frequency compared in the phase comparator circuit need not be the PLL output frequency. The logical frequency for comparison is 10 kHz, the common denominator of the desired output frequencies.

The phase comparator gives optimum comparison when comparing two waveforms of the same form. The two frequencies to be compared are available from the divide-by-N circuit and a 2 MHz crystal oscillator. The 2 MHz signal is divided by 400 to arrive at a frequency of 5 kHz and the output of the divide-by-N circuit is divided by 2 to provide

the other 5 kHz signal. Five kHz is used because the output of the divide-by-N circuit is a pulse, and a square wave is required.

The system block diagram is now that shwon in Fig. 8c.

C. THEORETICAL ANALYSIS AND DESIGN

The design of frequency discriminators is well documented and will not be discussed in this section. [Ref. 5] The frequency discriminators used in the MLFS are considered in detail in Appendix A.

The circuit requirements for the block labeled corrective circuit in Fig. 8a is found in the mathematical analysis of the control voltage loop. The transfer characteristic curve of control voltage V_A vs frequency f for the PLL (Fig. 9) can be closely approximated by the equation

$$f = \frac{10.42 - V_A}{3.34} \qquad (1)$$

where V_A is in volts and f is in MHz. The transfer characteristic curve of frequency vs output voltage V_o for the control voltage frequency discriminator (Fig. 10) can be closely approximated by the equation

$$V_o = 1.8f - 0.133 \qquad (2)$$

where V_o is in volts and f is in MHz. Substituting Eq. (1) into (2) and solving for V_A as a function of V_o gives

$$V_A = 9.975 - 1.85V_o. \qquad (3)$$

The corrective circuit must satisfy Eq. 3 with V_o as the input and V_A as the output. One such circuit that satisfies Eq. 3 is shown in Fig. 11.

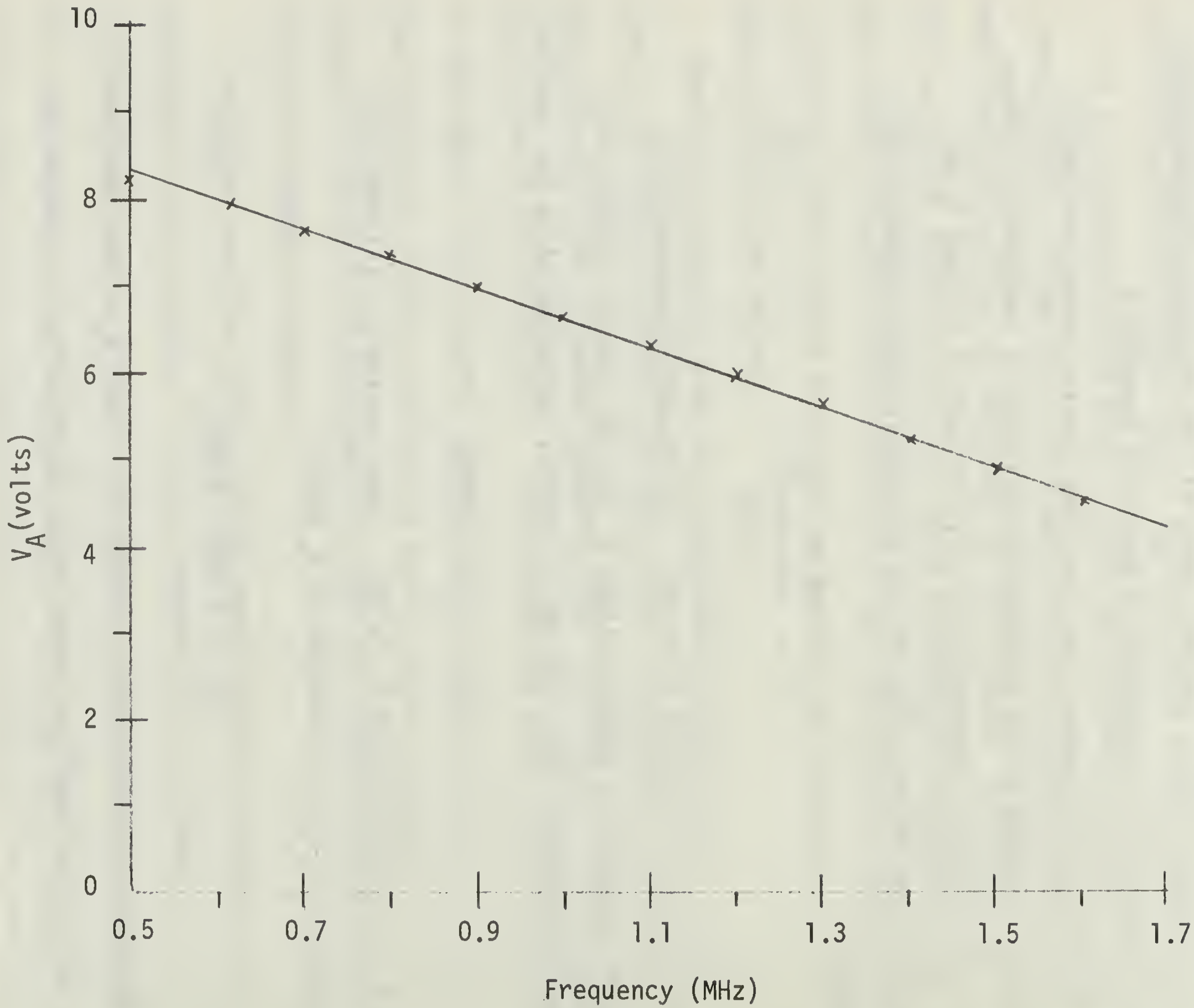


Fig. 9. PLOT OF CONTROL VOLTAGE V_A vs FREQUENCY f_o OF THE VCO OUTPUT VOLTAGE

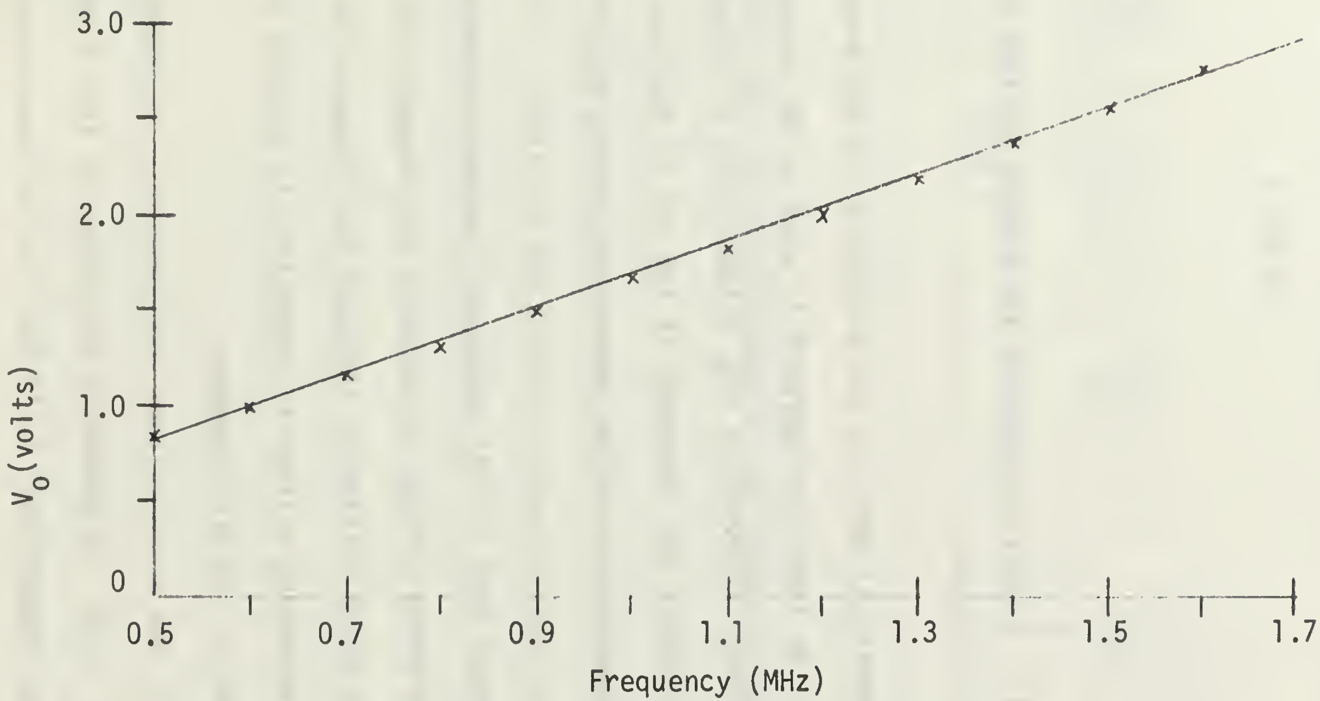


Fig. 10. PLOT OF THE DISCRIMINATOR OUTPUT VOLTAGE V_o vs FREQUENCY f_o OF THE VCO OUTPUT VOLTAGE.

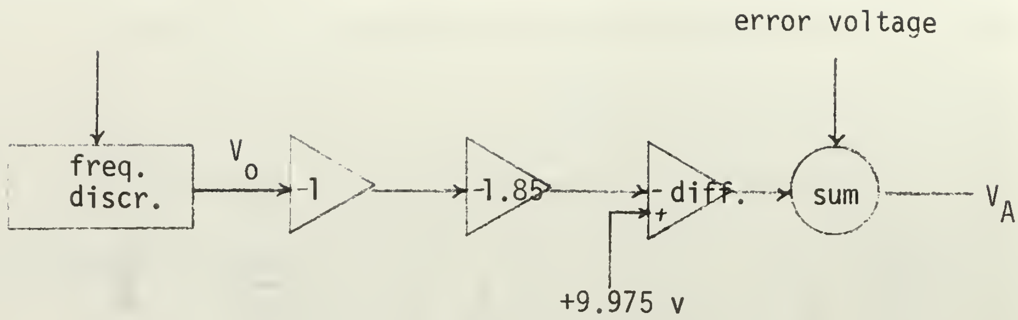


Fig. 11. CIRCUIT DIAGRAM OF THE CONTROL-VOLTAGE LOOP

Such a mathematical model is not available for the error-voltage loop; therefore, an intuitive approach is used in the design of the error-voltage loop. A review of Fig. 9 shows that an increase in control voltage causes the frequency of the PLL to decrease and vice versa. The desired output of the error-voltage loop shown in Fig. 8b is then

1. zero output when the PLL is exactly on the programmed frequency,
2. positive error voltage to decrease the frequency (on demand),
3. negative error voltage to increase the frequency (on demand), and
4. error correcting voltage to automatically correct large perturbations in the PLL frequency.

The output of the error-voltage loop frequency discriminator is proportional to f_o/N. By comparing the output of this discriminator with a DC voltage proportional to 10 kHz, the desired output of the

error-voltage loop is readily available. One possible circuit to accomplish this is shown in Fig. 12. A variable gain amplifier stage is included in the design. This allows the user to adjust the slew rate of the synthesizer.

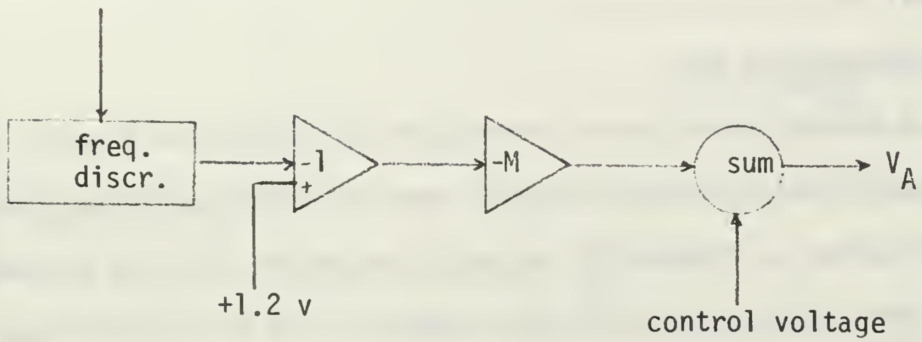


Fig. 12. CIRCUIT DIAGRAM OF THE ERROR-VOLTAGE LOOP

Design of the various subsystems of the MLFS is considered in the next chapter. Details of the circuit design of each stage of the synthesizer are presented in Appendix A.

IV. SUBSYSTEM DESIGN AND SYSTEM ALIGNMENT

A. SUBSYSTEM DESIGN

In this section we discuss briefly the design and performance of functional blocks of the MLFS with particular emphasis on the various loops of the system. See Fig. 1. Details of circuit design are given in Appendix A.

1. Phase-Locked Loop

We present here a brief description of the PLL in general, the voltage-controlled oscillator circuit, and the phase-comparator loop. This description is intended to acquaint the reader with the respective circuits only. A more detailed description of the PLL can be found in Ref. 6. The phase-comparator portion of the PLL is considered separately in part 5 of this section.

The PLL is a Signetics NE562 integrated circuit. Fig. 13 is a block diagram of this system. The NE562 is a complete monolithic PLL system designed for digital or analog circuit applications. It is particularly suited for signal conditioning and frequency synthesis applications (both frequency division and multiplication). The system has a provision for inserting a divide-by-N network into the frequency feedback path.

The VCO portion of the PLL is an emitter-coupled multivibrator. The VCO free-running frequency is determined by the timing capacitor C_0 connected across the terminals 5 and 6 shown in Fig. 13. Fig. 14 is the tuning characteristic curve used to select the value of C_0. The VCO free-running frequency can be changed by at least three octaves with the

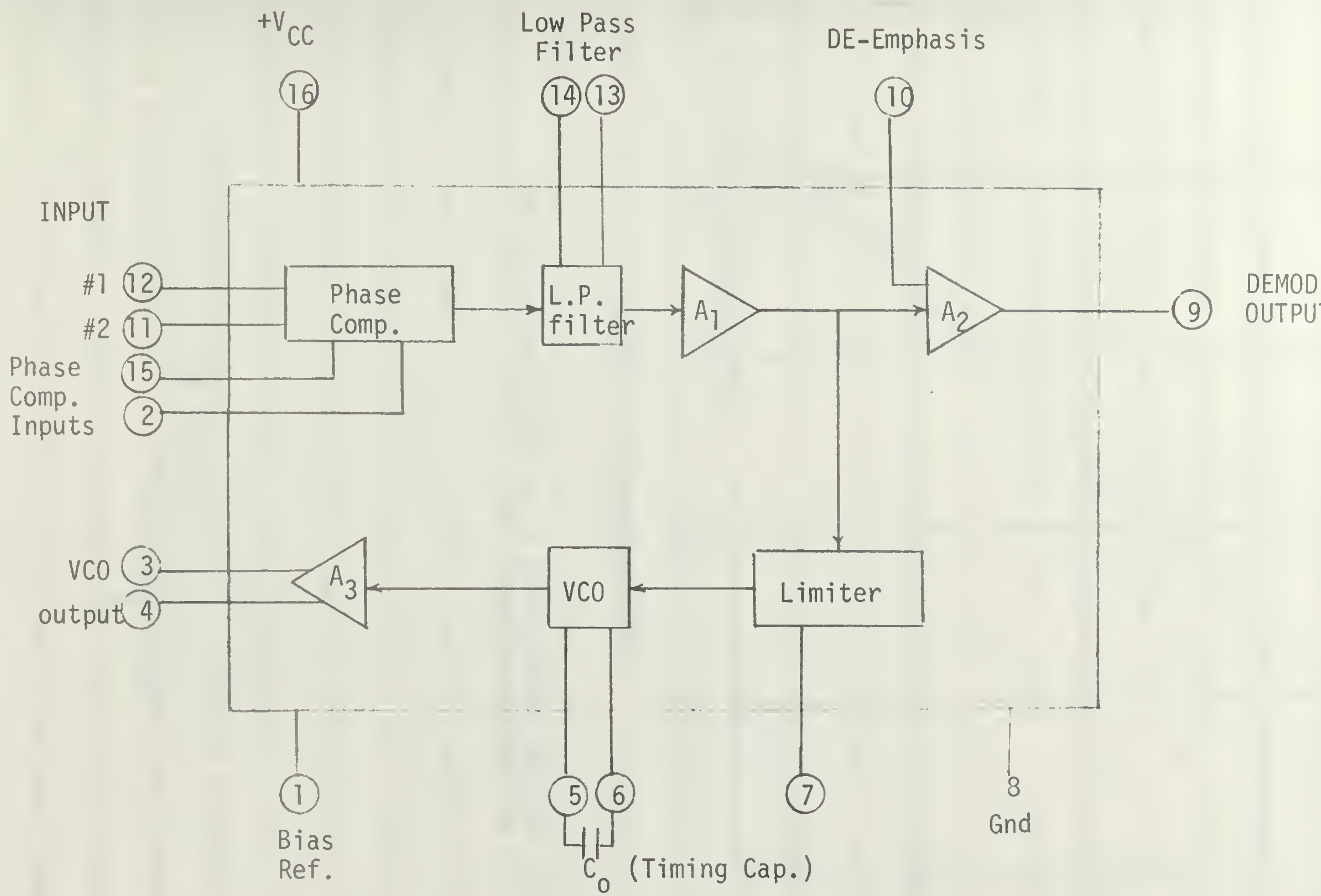


Fig. 13. BLOCK DIAGRAM OF THE PLL

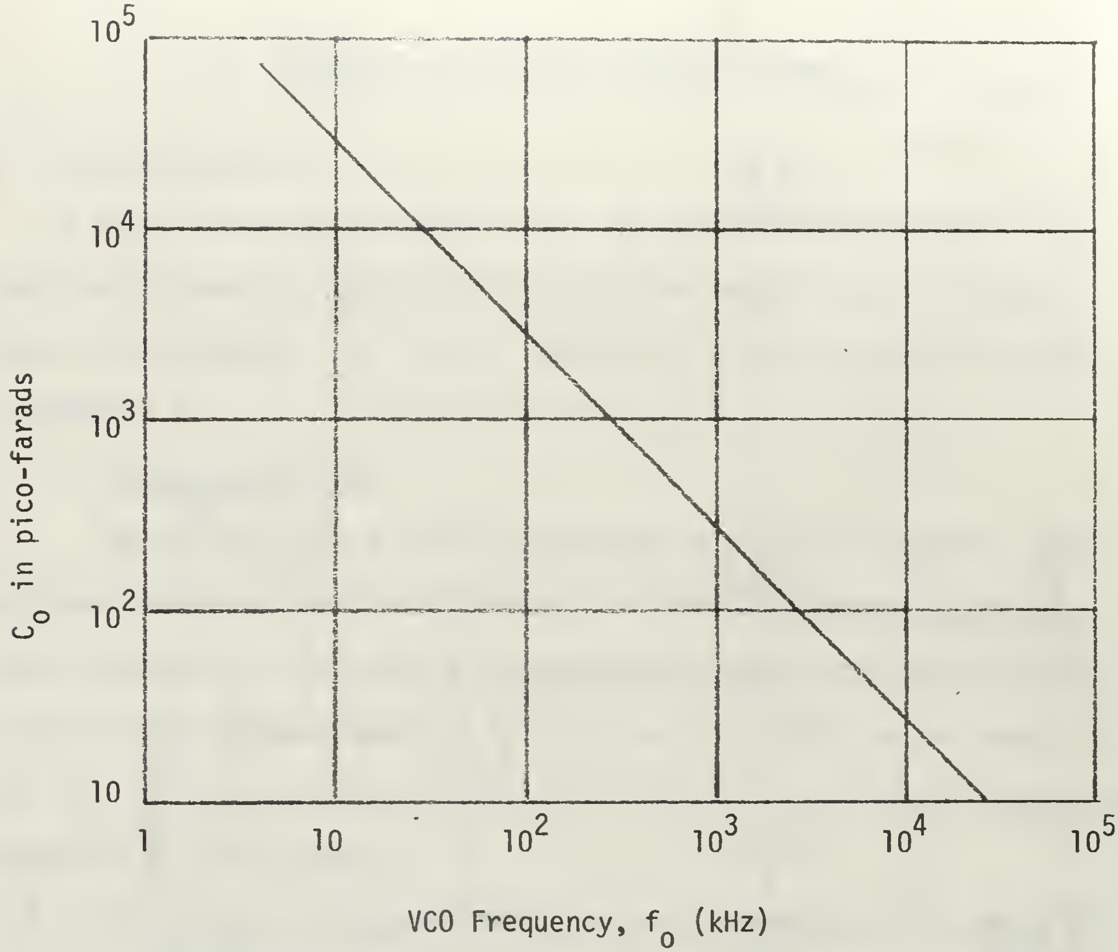


Fig. 14. PLOT OF CAPACITANCE C_o vs FREQUENCY f_o OF THE VCO OUTPUT VOLTAGE

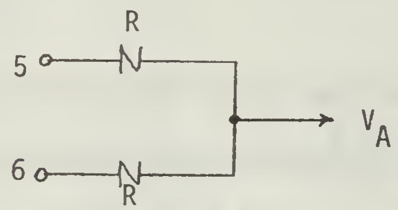


Fig. 15. VCO BIAS CIRCUIT DIAGRAM

application of an external voltage V_A by means of the external bias circuit shown in Fig. 15. The characteristic curve V_A vs frequency is shown in Fig. 9. A change of VCO frequency by an amount Δf from its original free-running frequency f_o to its fine-tuned frequency f_r can be closely approximated by the equation $\Delta f = \beta f_o(V_A - 6.4)/1.3R$. The new frequency is then given by the equation $f_r = f_o - \Delta f$ or $f_r = f_o(1 - \beta(V_A - 6.4)/1.3R)$ where V_A is in volts, R is in kΩ, and β is a unity constant having units of inverse amperes. When the VCO is at f_o the voltage at pins 5 and 6 is 6.4 volts. The bias circuit shown in Fig. 15 varies the charge and discharge time of C_0 by bleeding current out of or by inserting current into pins 5 and 6 depending on whether the change in frequency is positive or negative respectively.

2. Control Voltage Loop

The control voltage loop automatically generates the correct control voltage V_A for the programmed frequency. A Fairchild 9601 retriggerable one-shot multivibrator (IC) configured as a frequency discriminator is used to obtain a voltage proportional to the VCO output frequency. The transfer characteristic curve (frequency vs output voltage) for this discriminator is shown in Fig. 10. The balance of the control voltage loop operates on the frequency discriminator output voltage until it matches the VCO voltage requirements shown in Fig. 9.

The voltage characteristic of Fig. 10 can be matched to that of Fig. 9 by first rotating the curve of Fig. 10 about the frequency axis, then multiplying by a factor M to match the slope of the curve in Fig. 9, and then linearly translating the resulting curve upward to match that of Fig. 9. The sequence of operation is shown in Fig. 16. Fig. 16 is merely a model set of curves and not the actual curves represented by Figs. 9 and 10.

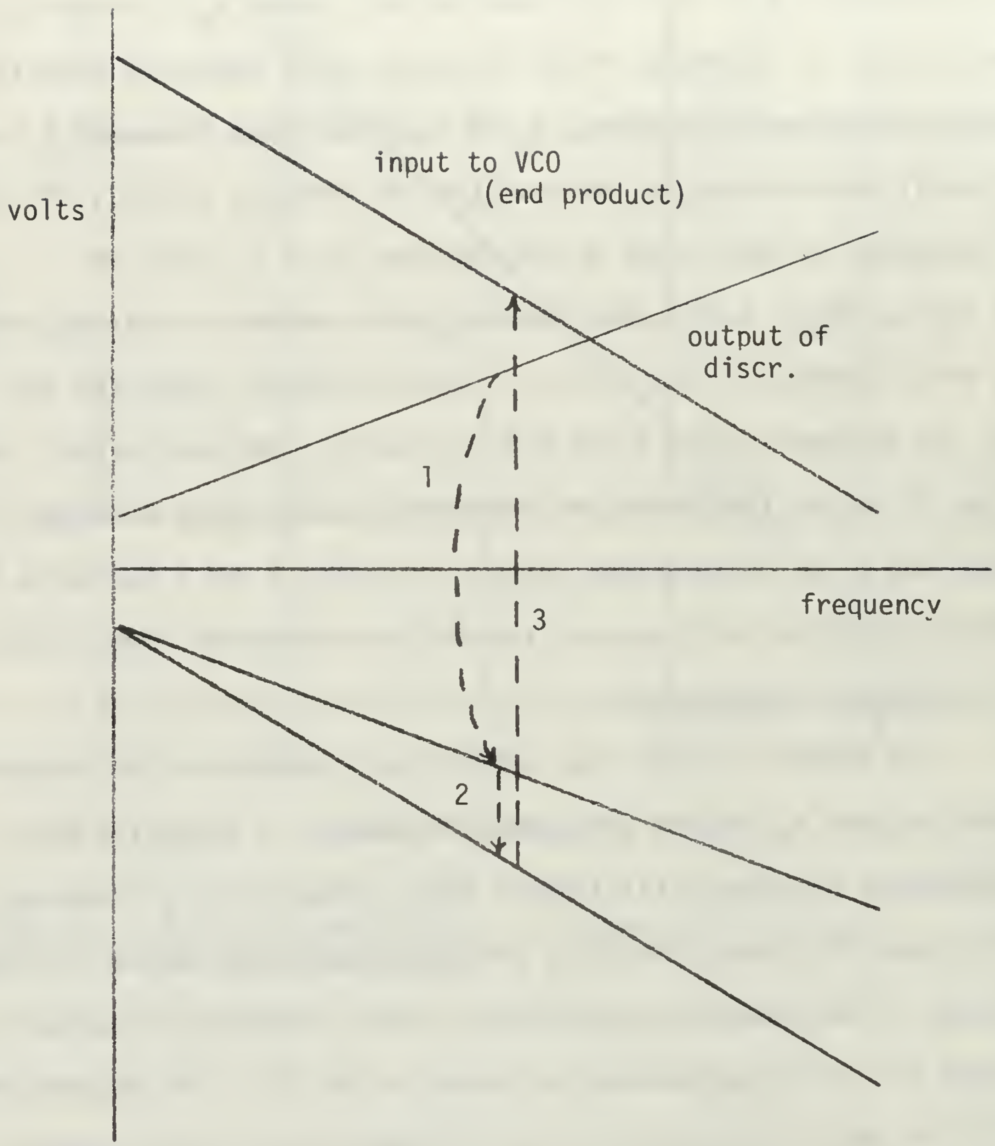


Fig. 16. MODEL SET OF CURVES SHOWING THE TRANSLATION OF THE DISCRIMINATOR OUTPUT VOLTAGE V_o TO THE VCO CONTROL VOLTAGE V_A.

3. Divide-By-N Circuit

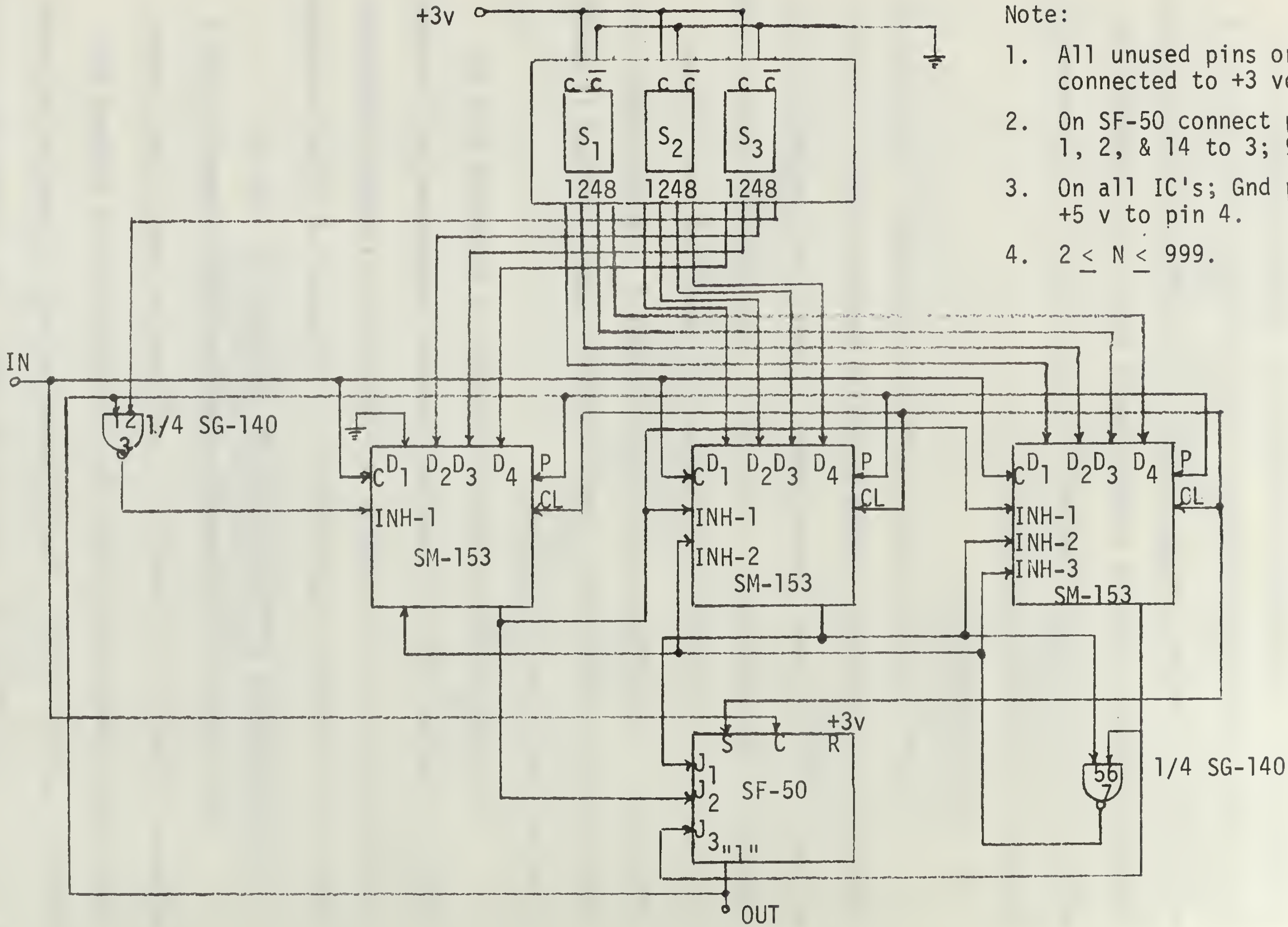
The divide-by-N circuit is a 3-digit programmable divider of Sylvania design. The divider is capable of frequency division by $2 \leq N \leq 999$ with an upper frequency limit of 20 MHz. The value of N and the output frequency of the synthesizer is programmed by a BCD rotary thumbwheel switch. When the synthesizer is exactly as programmed the output of the divide-by-N circuit is 10 kHz. Fig. 17 is the schematic diagram of the divide-by-N circuit.

4. Error Voltage Loop

The error voltage loop performs two functions. It provides the forcing function (voltage) needed to change frequency, and it corrects any large errors between the programmed frequency and the actual output frequency of the synthesizer. From Fig. 9, note that the control voltage must decrease to increase the frequency. On the other hand, if the synthesizer is programmed to generate frequency f_o and then there is a sudden increase in frequency, a more positive control voltage is needed to correct the error in frequency.

The output of the divide-by-N circuit is converted to a DC voltage by another 9601 retriggerable one-shot configured as a frequency discriminator. Fig. 18 is output voltage vs input frequency characteristic of this frequency discriminator. A frequency of 10 kHz corresponds to an output voltage of +1.2 volts, for example.

The frequency discriminator output voltage is compared with a reference voltage of +1.2 volts in a differencing circuit which translates downward the curve in Fig. 18 such that the curve crosses the frequency axis at 10 kHz. The difference voltage is then multiplied by a factor K to increase the slope of the curve. The voltage at this point is labeled error voltage V_E. Fig. 19 is a plot of V_E vs frequency.



Note:

1. All unused pins on SM-153 connected to +3 volts
2. On SF-50 connect pins 1, 2, & 14 to 3; 9 to 12.
3. On all IC's; Gnd pin 10, +5 v to pin 4.
4. $2 \leq N \leq 999$.

Fig. 17. DIAGRAM OF THE DIVIDE-BY-N CIRCUIT

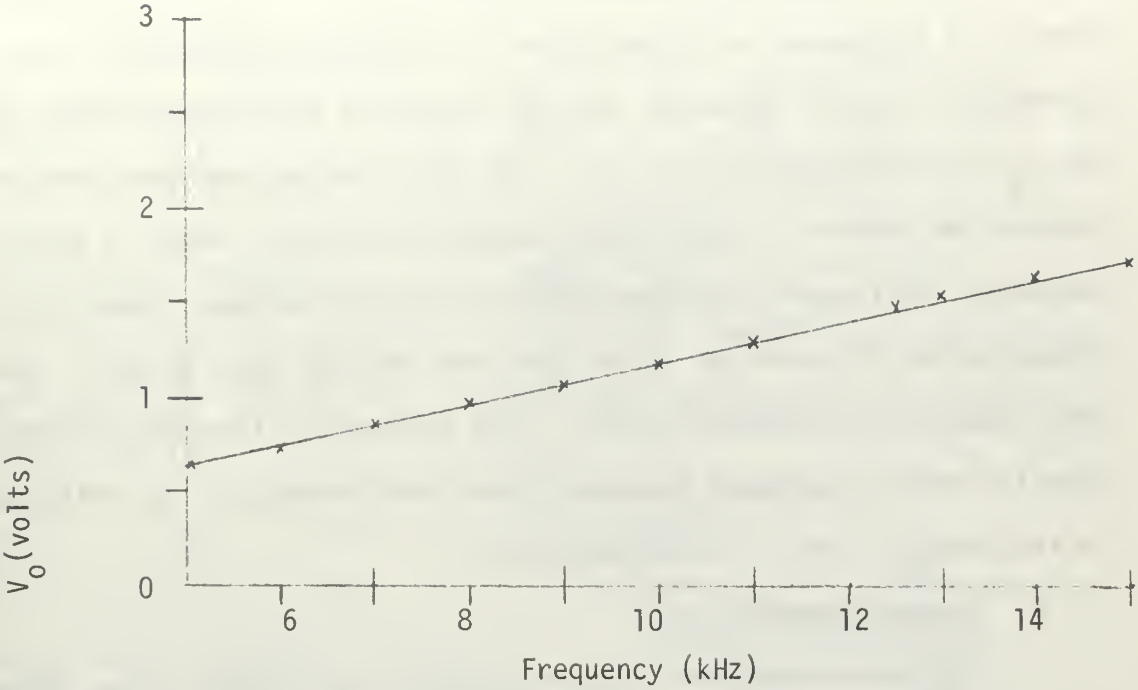


Fig. 18. PLOT OF THE DISCRIMINATOR OUTPUT VOLTAGE V_O vs FREQUENCY f_o/N OF THE DIVIDE-BY-N CIRCUIT OUTPUT VOLTAGE

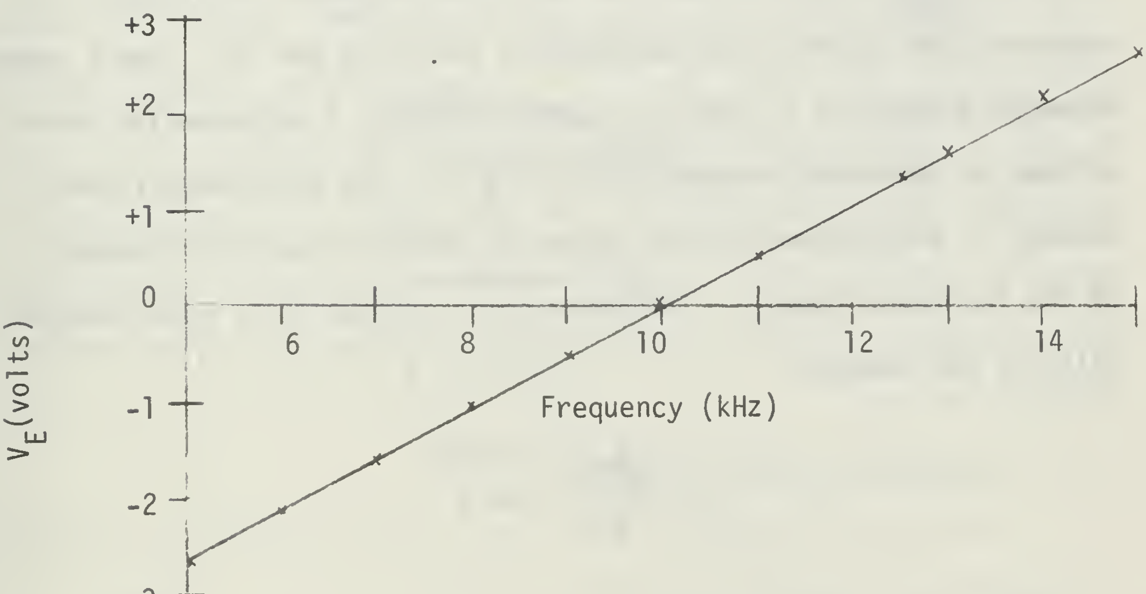


Fig. 19. PLOT OF THE ERROR VOLTAGE V_E vs FREQUENCY f_o/N OF THE DIVIDE-BY-N CIRCUIT OUTPUT VOLTAGE

To increase the programmed frequency by 10 kHz the divide-by-N circuit is programmed to divide by N+1. The output frequency of the divide-by-N circuit decreases thereby decreasing the output voltage of the f_o/N discriminator in Fig. 20. The error voltage now goes negative forcing the control voltage in the negative direction, which in turn increases the frequency of the synthesizer output voltage. When this frequency has increased by 10 kHz the error voltage goes to zero. The same sequence of operation occurs if the synthesizer frequency differs from the exact programmed frequency since this change will be reflected in the output of the divide-by-N circuit.

5. Phase-Comparator Loop

The phase-comparator loop functions as an automatic fine tuning circuit. This loop is internal to the phase-locked loop and is comprised of the phase-comparator, low pass filter and Amplifier A_1 of Fig. 13.

The phase-comparator is a doubly balanced multiplier circuit. The inputs are 5 kHz derived from the 2 MHz reference oscillator connected to pin 15 and $f_o/2N$ connected to pin 12 of the IC. When a doubly balanced multiplier is used as a phase detector, a differential error voltage is developed between pins 13 and 14. The differential error voltage is proportioned to the cosine of the phase angle difference θ of the two input signals. The phase error voltage V_d is given analytically by the equation:

$$V_d = \frac{I_B R q E_s}{k\,T} \cos\theta$$

where: k = Boltzmann constant

q = electronic charge

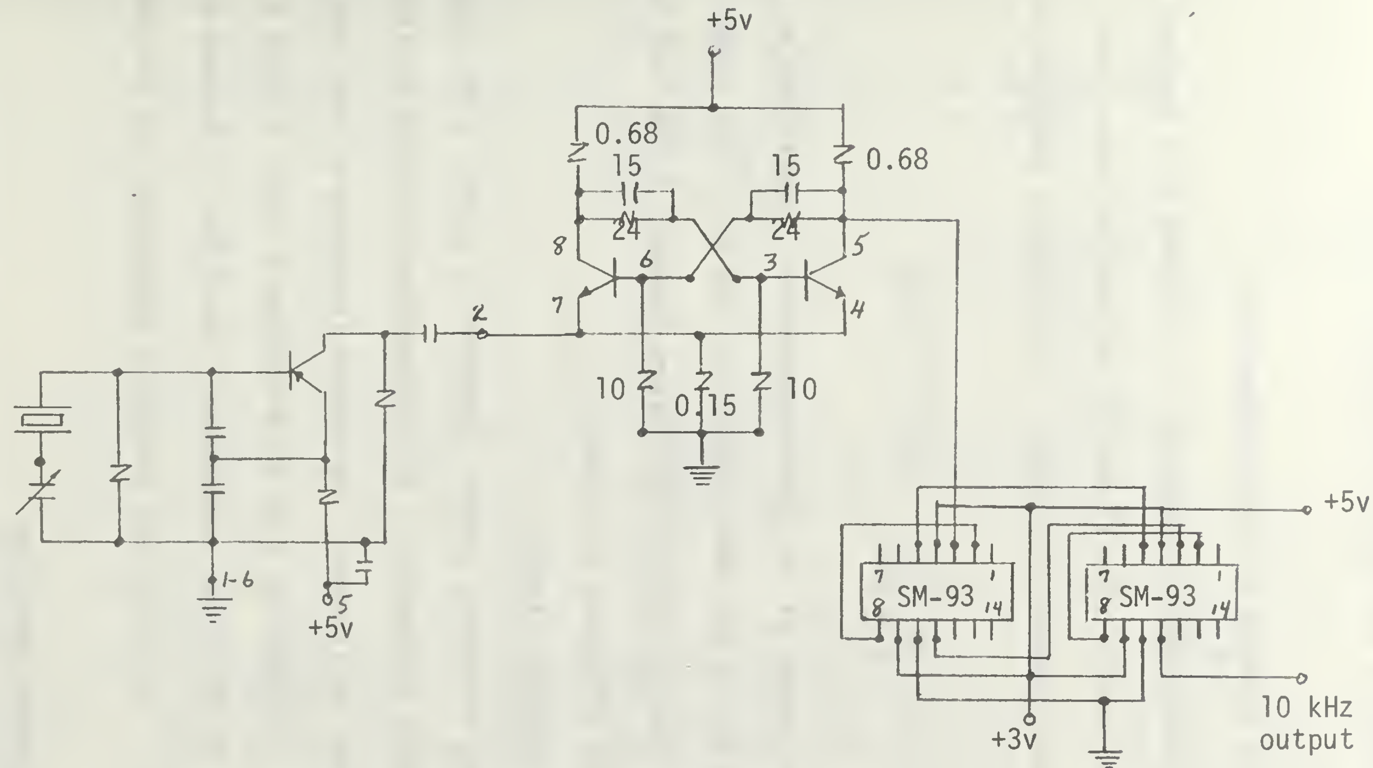


Fig. 20. CIRCUIT DIAGRAM OF THE 10 kHz STABLE REFERENCE SOURCE

T = temperature in °K

E_s = amplitude of the signal of frequency $f_o/2N$

R = 6 kΩ

I_B = current through the phase comparator.

The output of the phase-comparator is filtered by a lowpass filter formed by a capacitor across pins 13 and 14 and the collector load resistors in the phase-comparator circuit. The transfer function of this filter is

$$F(s) = \frac{1}{1 + 2sRC} \quad \text{where } R = 6\ \text{k}\Omega$$

The filtered output of the phase-comparator is amplified by the DC amplifier A_1 in Fig. 13 and then fed back to the VCO. The error voltage adjusts the bias to correct for errors between $f_o/2N$ and the 5 kHz signal from the reference oscillator.

6. Reference Frequency Circuit

The reference frequency circuit generates a stable 5 kHz signal to be used in the phase comparator. An International Crystal oscillator is used as a reference oscillator. The output frequency of the crystal oscillator is 2 MHz ± 0.0025% or ± 50 Hz providing a 5 kHz ± 0.125 Hz signal at the input of the phase comparator. The 2 MHz is divided by 400 to obtain 5 kHz. Fig. 20 is the schematic diagram of the reference frequency circuit.

7. Integrated System Operation

Fig. 21 is a block diagram of the complete frequency synthesizer. The complete schematic of the MLFS is shown in Fig. 22. The total system operation combines the individual subsystem operations described in sections A1 through A6 of this chapter.

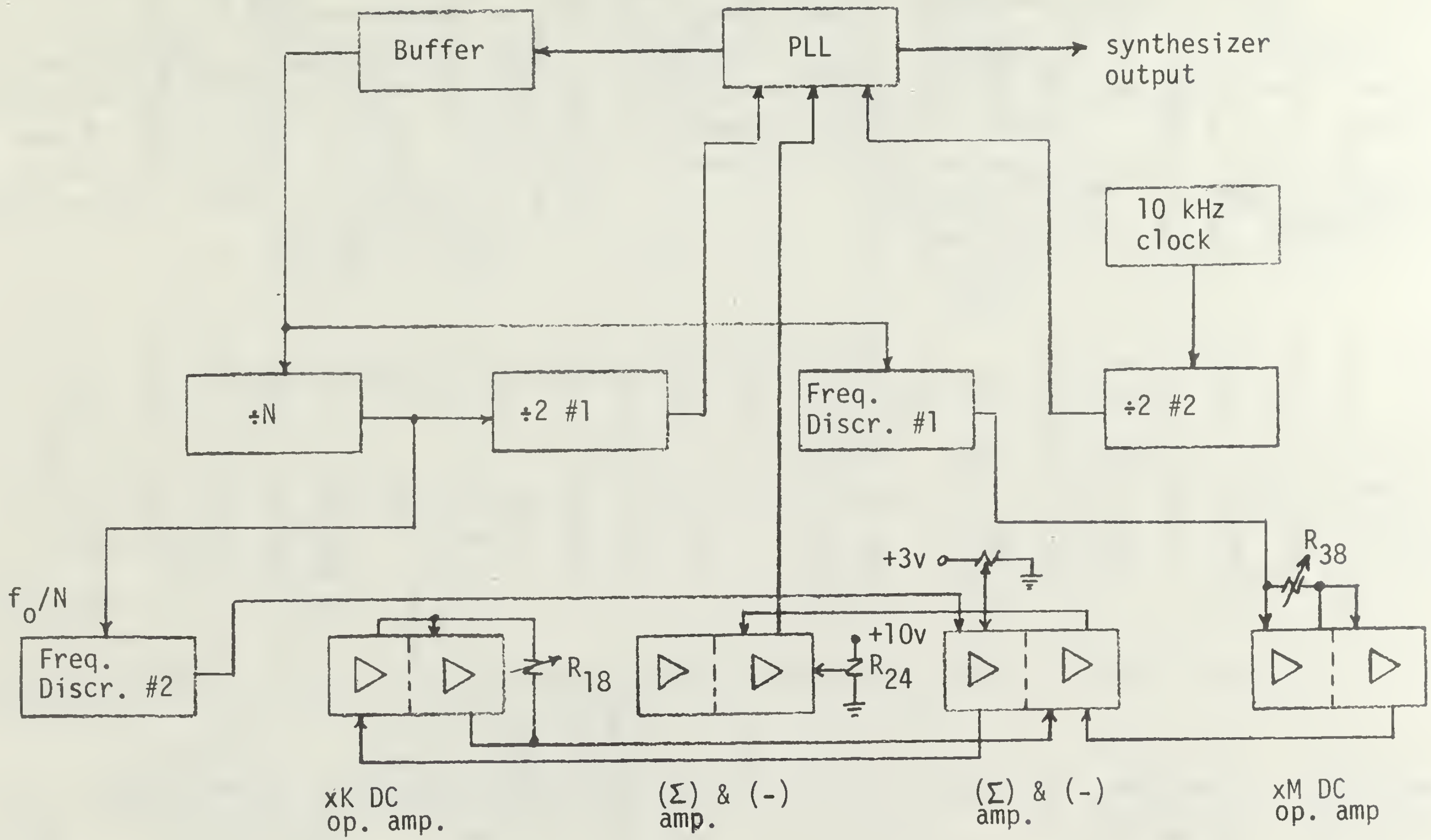


Fig. 21. BLOCK DIAGRAM OF THE MLFS

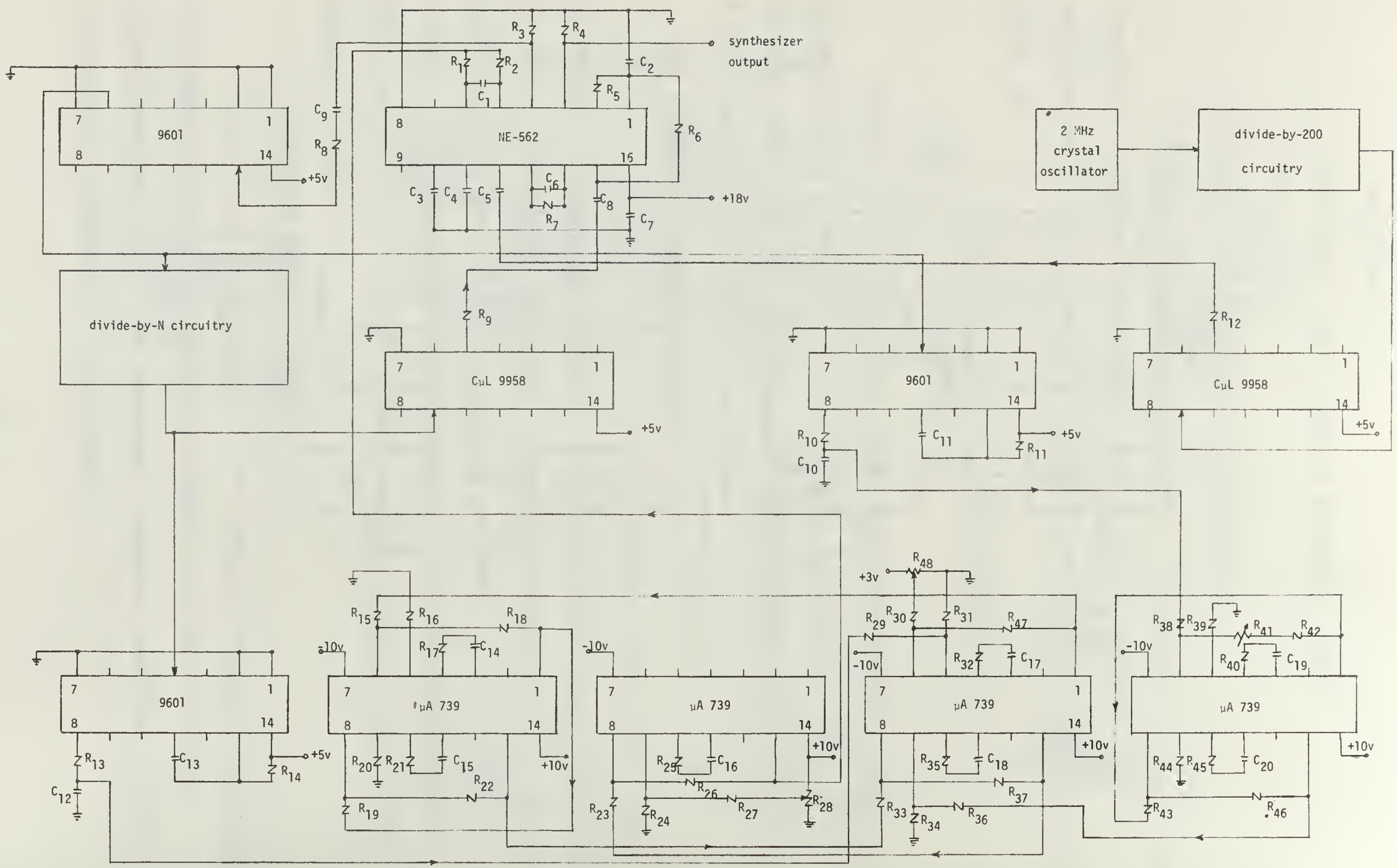


Fig. 22. CIRCUIT DIAGRAM OF THE MLFS

List of Values of Components Shown in Fig. 22.

R_1 = 4.7 kΩ	R_{24} = 1.1 MΩ	R_{47} = 1.1 MΩ
R_2 = 4.7 kΩ	R_{25} = 5.1 Ω	R_{48} = 10 kΩ
R_3 = 12 kΩ	R_{26} = 1.1 MΩ	C_1 = 390 pF
R_4 = 12 kΩ	R_{27} = 1.1 MΩ	C_2 = 1.05 μF
R_5 = 1 kΩ	R_{28} = 10 kΩ	C_3 = 1.05 μF
R_6 = 1 kΩ	R_{29} = 1.1 MΩ	C_4 = 1.05 μF
R_7 = 750 Ω	R_{30} = 1.1 MΩ	C_5 = 0.1 μF
R_8 = 10 kΩ	R_{31} = 1.1 MΩ	C_6 = 0.1 μF
R_9 = 22 kΩ	R_{32} = 5.1 Ω	C_7 = 1.05 μF
R_{10} = 1 kΩ	R_{33} = 1.1 MΩ	C_8 = 0.1 μF
R_{11} = 10 kΩ	R_{34} = 1.1 MΩ	C_9 = 0.1 μF
R_{12} = 1.5 kΩ	R_{35} = 5.1 Ω	C_{10} = 1.05 μF
R_{13} = 10 kΩ	R_{36} = 1.1 MΩ	C_{11} = 100 pF
R_{14} = 30 kΩ	R_{37} = 1.1 MΩ	C_{12} = 1.05 μF
R_{15} = 1.1 MΩ	R_{38} = 1.1 MΩ	C_{13} = 0.0022 μF
R_{16} = 560 kΩ	R_{39} = 560 kΩ	C_{14} = 0.1 μF
R_{17} = 5.1 Ω	R_{40} = 5.1 Ω	C_{15} = 0.1 μF
R_{18} = 1.1 MΩ	R_{41} = 5 MΩ	C_{16} = 0.1 μF
R_{19} = 1.1 MΩ	R_{42} = 1.1 MΩ	C_{17} = 0.1 μF
R_{20} = 1.1 MΩ	R_{43} = 1.1 MΩ	C_{18} = 0.1 μF
R_{21} = 5.1 Ω	R_{44} = 560 kΩ	C_{19} = 0.1 μF
R_{22} = 1.85 MΩ	R_{45} = 5.1 Ω	C_{20} = 0.1 μF
R_{23} = 1.1 MΩ	R_{46} = 1.1 MΩ	

The desired output frequency is programmed in the divide-by-N circuit by appropriately setting the BCD switch. The synthesizer frequency is read directly on the switch. The synthesizer frequency is sampled by the divide-by-N circuit and the voltage control loop. The voltage control loop provides the correct voltage required by the VCO to produce the desired frequency of the output signal.

The error voltage loop samples the divide-by-N circuit frequency and determines if the synthesizer frequency is as programmed. If not, an error voltage is added to the control voltage to correct the frequency. When the synthesizer frequency is as programmed the error voltage goes to zero.

The output frequency of the divide-by-N circuit is divided by two and returned to the phase-comparator circuit to be compared with a reference frequency to obtain the proper phase. A phase error voltage is generated and applied to the bias circuit of the VCO which locks the VCO in phase with the reference frequency.

B. SYSTEM ALIGNMENT

There are three possible adjustments in the synthesizer: (1) zero error, (2) control voltage DC offset, and (3) control voltage slope adjust. A slew rate adjustment was eliminated. Tests show that a gain of K = 2 in the error voltage loop is required to optimize the slew rate and still maintain a suitable gain margin. An increase of the gain causes instability, and a decrease in gain makes the system sluggish. A gain of 2 is designed into the system.

The zero error adjustment is a critical adjustment and must be performed before any other meaningful adjustments can be made. Best

results are obtained if the following procedure is followed:

(1) remove the PLL (NE562),

(2) jumper the 100 kHz frequency signal from the output of the flip-flop in the 10 kHz reference circuit into the output pin of the PLL socket,

(3) program the synthesizer to read 010 on the switch face. This will provide 10 kHz out of the divide-by-N circuit,

(4) connect a VTVM to pin 13 of DC operational amplifier number 4,

(5) adjust the "Zero Error Adjust" R_{25} in Fig. 22 for a zero reading on the VTVM,

(6) remove the 100 kHz jumper, replace the PLL, and remove the VTVM.

The output of the PLL cannot be used to make this adjustment because every change made with this control will change the PLL frequency. The results will be a continuous adjustment with no success.

The control voltage DC OFFSET linearly shifts the output of the control-voltage frequency discriminator as indicated by step 3 in Fig. 15. The control voltage SLOPE CONTROL changes the gain of the control-voltage loop and affects the control voltage as shown in step 2 in Fig. 16. These two controls must be adjusted alternately. The most effective method of adjustment is:

(1) program the synthesizer for an output signal frequency of 500 kHz (050, on the switch),

(2) connect the VTVM to read voltage V_A at the junction of R_1 and R_2 or pin 13 of DC operational amplifier number 3,

(3) connect a frequency counter to the MLFS output,

(4) adjust R_{24} "DC OFFSET" for a voltage V_A corresponding to 500 kHz in Fig. 9,

(5) program the synthesizer for 1500 kHz (150, on the switch),

(6) adjust R_{38} "SLOPE CONTROL" until V_A is the value indicated in Fig. 9 for a frequency of 1500 kHz,

(7) repeat steps (4) and (5) until no adjustment is necessary to maintain the prescribed voltages,

(8) step the synthesizer completely through its frequency range from 500 kHz to 1600 kHz to insure proper alignment.

V. CONCLUSIONS AND RECOMMENDATIONS

The MLFS was designed, built and tested and found to operate very well although the spurious output level is relatively large. A respectable spurious level is of the order of -60 db. It is felt that with some additional engineering and packaging effort this level could be obtained. In the design, frequency stability problems were expected since the use of voltage control loops are supposedly unsuitable for frequency synthesizer control.

Frequency stability required in synthesizers cannot be obtained using voltage control loops alone; however they can be used as a coarse frequency control. The MLFS uses a phase comparator loop for fine frequency control. The marriage of voltage control loops, for coarse frequency control, and a phase comparator loop, for fine frequency control, provides the required frequency stability. Problems with radio-frequency interference were not expected at the frequencies utilized in the MLFS. However some considerable effort was required to shield and isolate components to reduce this interference to a tolerable level.

An improved version of the existing MLFS might incorporate the following changes: (1) reduce the component count by replacing the two CμL9958's with one 9020 (dual J-K flip-flop), the flip-flop in the reference source circuit with a 9001 flip-flop, two 9601's with one 9602 (dual 9601), and the four μA739's with two quad DC operational amplifier circuits, (2) use a separate ground bus for digital and analog circuits, (3) select a 1 MHz crystal oscillator to replace the 2 MHz crystal oscillator and (4) improve the isolation between digital and analog circuits.

APPENDIX A

DISCRETE STAGE DESIGN

This appendix presents the design, in detail, for all discrete stages used in the Multiple-Loop Frequency Synthesizer.

Circuitry for the PLL will be developed first, followed by the design of both frequency discriminators. DC operational amplifier design will be discussed showing the various modes of operation used in the synthesizer. The last two sections of this Appendix will cover the design of the divide-by-N circuit and the stable reference source.

A. PLL CIRCUIT

General characteristics for the PLL (NE-562) are given in Table A-1.

TABLE A-1 NE-562 GENERAL CHARACTERISTICS

Unless otherwise specified V_{cc} = +18V and T_A = 25°C

Characteristic	Min.	Typ.	Max	Units
V_{cc}	15	18	24	volts
Upper frequency limit	15	30		MHz
Lower frequency limit		0.1		Hz
Supply current		12	14	ma
Dynamic range		80		db
Minimum input signal		200		μV
Frequency drift vs temp		±0.06	±0.15	%/°C
Frequency drift vs power supply		±0.03	±2	%/volt
Tracking range	±5	±20		% of f_o
Input resistance		2		kΩ
Input capacitance		4		pF
Input DC level		4		volts
VCO output impedence		1.3	2.5	kΩ
VCO output swing	3	4.5		volts peak-to-peak
VCO output DC level		12		volts
VCO signal/noise ratio		60		db

Fig. A-1 is the schematic diagram of the PLL circuit. Resistors R_3 and R_4 are the values recommended by the manufacturer for proper loading of the output differential amplifier. Capacitors C_2, C_3, C_4, and C_7 are bypass capacitors and capacitors C_5 and C_8 are coupling capacitors. Capacitor C_6 and R_7 together with the internal resistance between pins 13 and 14 form the lowpass filter at the output of the phase comparator. The lowpass filter transfer function is given by equation A-1 where R is the parallel combination of R_7=750Ω and 6 kΩ, the internal resistance between pins 13 and 14.

$$F(s) = \frac{1}{1 + 2sRC_6} = \frac{1}{1 + 1.33s \times 10^{-4}} \qquad \text{(A-1)}$$

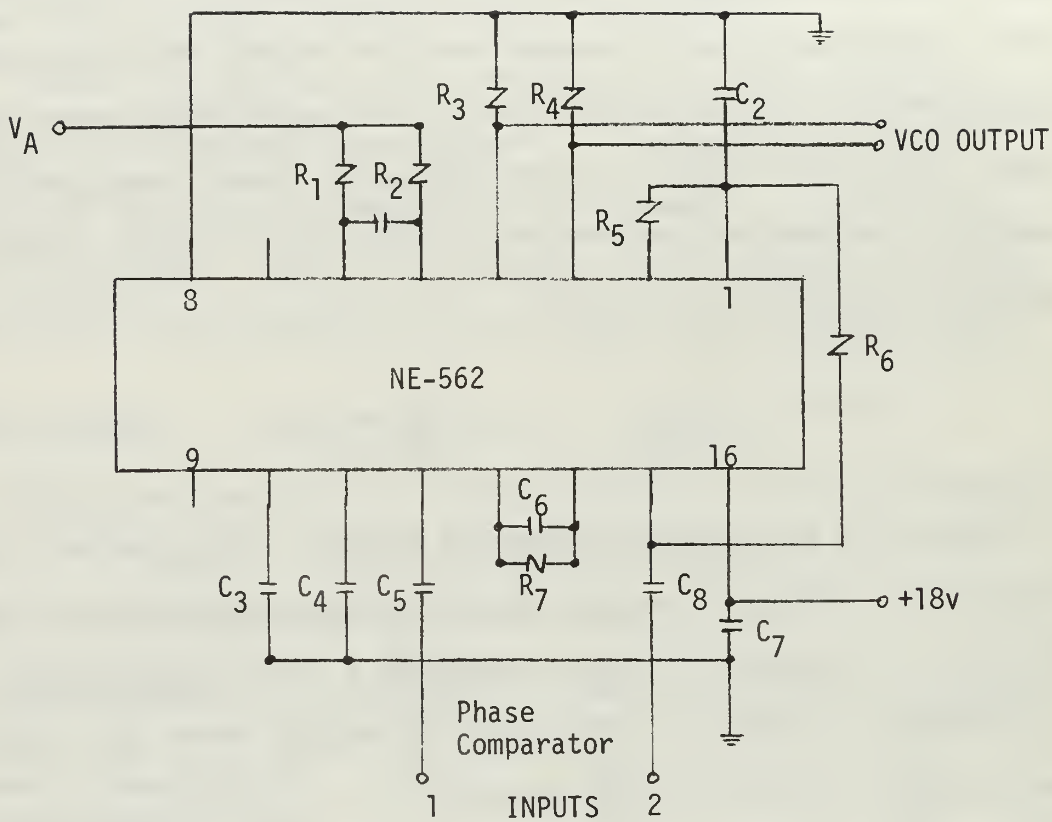
Resistor R_7 was connected across the low-pass filter terminals (pins 13 and 14) to reduce the overall gain and detection sensitivity of the PLL. The gain and sensitivity is reduced by a factor α where $\alpha < 1$.

Equation A-1 expresses α in terms of R_7 and R_A, where R_A = 6 kΩ the impedance looking into Pins 13 and 14.

$$\alpha = \frac{R_7}{2\ R_A + R_7} = \frac{750}{12{,}000 + 750} = 0.0588 \qquad \text{(A-2)}$$

Capacitor C_1 was selected, using Fig. 14, to make the free-running frequency just below 1.0 MHz. Resistors R_1 and R_2 ($R_1 = R_2$ = 4.7 kΩ) were selected to satisfy Eq. A-3 below. In Eq. A-3, β is unity, V_A corresponds to a deviation Δf from f_o as given by Fig. 9. The frequency f_o corresponds to a value of V_A = 6.4 volts.

$$\Delta f = \beta f_o\ (V_A - 6.4)/1.3R_1 \qquad \text{(A-3)}$$



$R_1 = 4.7\ k\Omega$	$C_1 = 390\ pF$
$R_2 = 4.7\ k\Omega$	$C_2 = 1.05\ \mu F$
$R_3 = 12\ k\Omega$	$C_3 = 1.05\ \mu F$
$R_4 = 12\ k\Omega$	$C_4 = 1.05\ \mu F$
$R_5 = 1\ k\Omega$	$C_5 = 0.1\ \mu F$
$R_6 = 1\ k\Omega$	$C_6 = 0.1\ \mu F$
$R_7 = 750\ \Omega$	$C_7 = 1.05\ \mu F$
	$C_8 = 0.1\ \mu F$

Fig. A-1. CIRCUIT DIAGRAM OF THE PLL

B. FREQUENCY DISCRIMINATORS

Two different frequency discriminators of the same basic design are used in the MLFS. The design used is shown in Fig. A-2. This design is taken from Fairchild application note No. 173. A simple resistor-capacitor integration network, on the output of the retriggerable one-shot (9601), was used to produce a linear output voltage proportional to the input frequency. The frequency range of operation is determined by R_x and C_x.

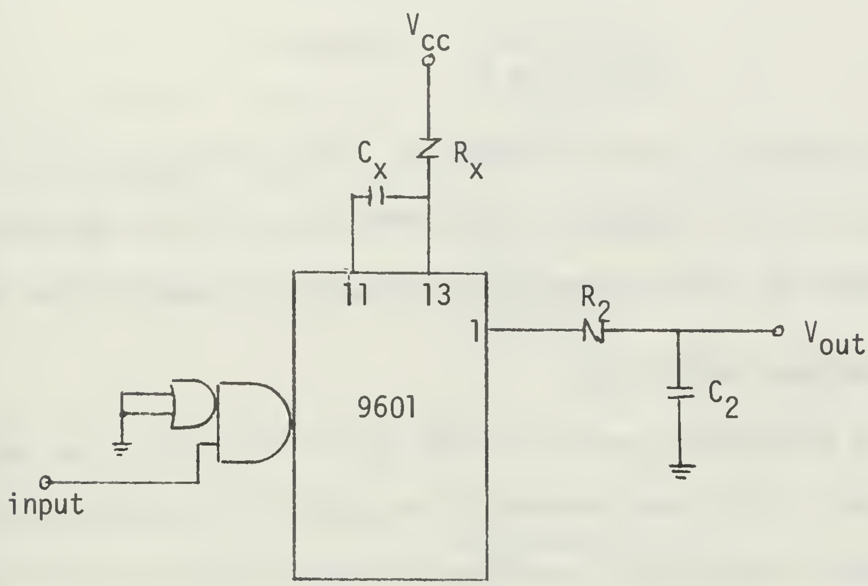


Fig. A-2. CIRCUIT DIAGRAM OF THE DISCRIMINATOR

The maximum output voltage for the circuit of Fig. A-2 is +4 volts. In the design of the frequency discriminator having center frequency f_o, let f = 2 MHz. Then the period T = $1/2 \times 10^6$ = 500 nsec. Let R_x = 10 kΩ. Then from Fig. 14, Page 3 - 111 of Ref. 7, C_x = 100 pF. We desire $R_2C_2 \leq 1 \times 10^{-3}$. Let $R_2C_2 = 1 \times 10^{-3}$. Then R_2 = 1 kΩ and C_2 = 1 μF.

The characteristic transfer curve of frequency vs output voltage for this frequency discriminator is shown in Fig. 10. In the design of the frequency discriminator having center frequency f_o/N, let f_{max} = 20 kHz. The corresponding period $T = 1/4 \times 10^4$ = 25,000 nsec. From Ref. 7,

$$T = 0.32C_x(R_x + 0.7) \tag{A-4}$$

where R_x is in kΩ, C_x is in pFd, and T is in nsec. Let R_x = 30 kΩ. Then solving Eq. A-4 for C_x gives

$$C_x = \frac{2.5 \times 10^4}{(0.32)\ (30.7)} = 2544\ \mu F.$$

The actual value of C_x used is 0.0022 μF. We desire $R_2C_2 \leq 1 \times 10^{-1}$. Let $R_2C_2 = 1 \times 10^{-1}$. Then R_2 = 10 kΩ and C_2 = 1 μF. The characteristic transfer curve for this frequency discriminator is shown in Fig. 18.

C. DC OPERATIONAL AMPLIFIERS

Eight DC operational amplifiers are used in the MLFS. The μA739 (dual op. amp.) IC is used throughout the design. The three amplifier configurations used are (1) inverting unity gain amplifier, (2) inverting variable gain amplifier and (3) sum and difference amplifier. Fig. A-3 shows the three amplifier configurations used. Frequency compensation circuits are connected between pins 3 and 4 and 10 and 11. The frequency compensation network is the same for all amplifiers and is a 5.1Ω resistor in series with a 0.1 μF capacitor. The value of the resistors labeled R in Fig. A-3 is 1.1 MΩ.

The gain of the inverting variable gain amplifier is given by $|A| = \left|1 + \frac{R_F}{R}\right|$ where R_F is a variable resistance and the braces denote magnitude.

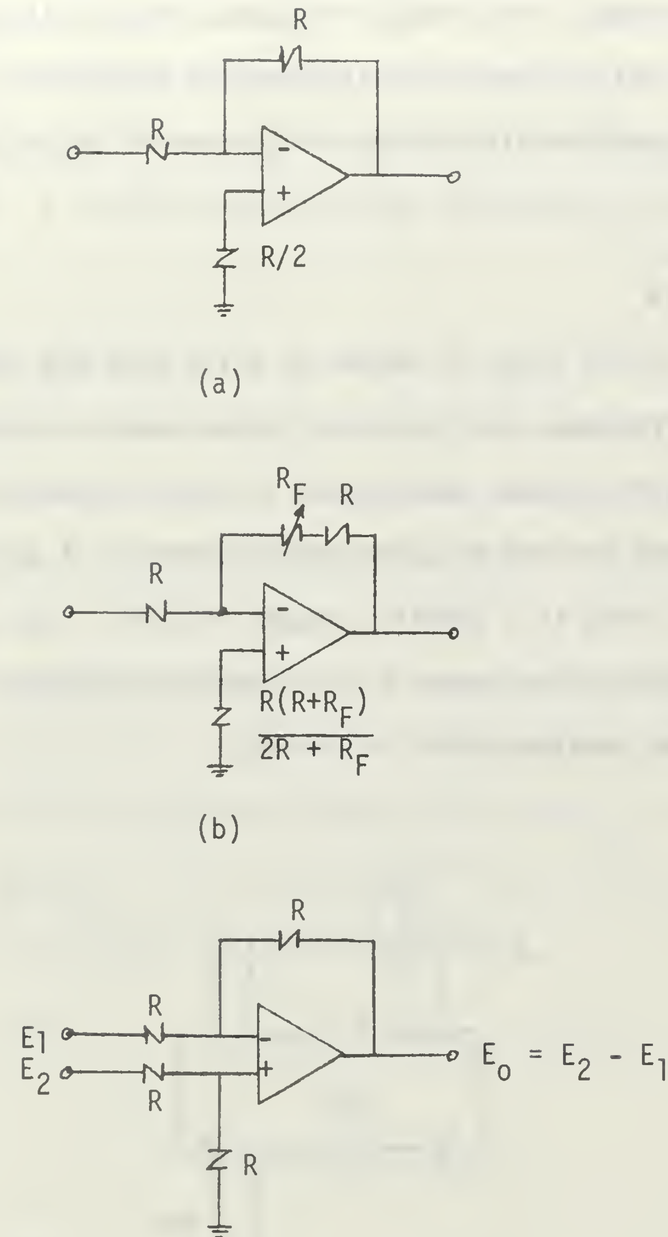


Fig. A-3. DC OPERATIONAL AMPLIFIER CONFIGURATIONS
(a) inverting unity gain amplifier, (b) inverting variable gain amplifier, (c) sum/difference amplifier.

DC operational amplifiers require the impedance as seen by the inverting and non-inverting input terminals of the operational amplifier to be matched. This reduces the zero offset voltage at the output. In the MLFS this is not critical since any zero offset voltage in the system can be cancelled with either the zero-error adjust or DC offset adjust control.

D. BUFFER

One buffer stage is needed to drive both the divide-by-N circuit and the frequency discriminator in the control voltage loop. This is necessary to prevent loading the PLL and to generate a constant amplitude signal for the frequency discriminator. A retriggerable one-shot (9601) is used as a Schmitt trigger circuit. Fig. A-4 is the schematic of the buffer stage where C is a coupling capacitor and R is used to reduce the loading effect on the PLL.

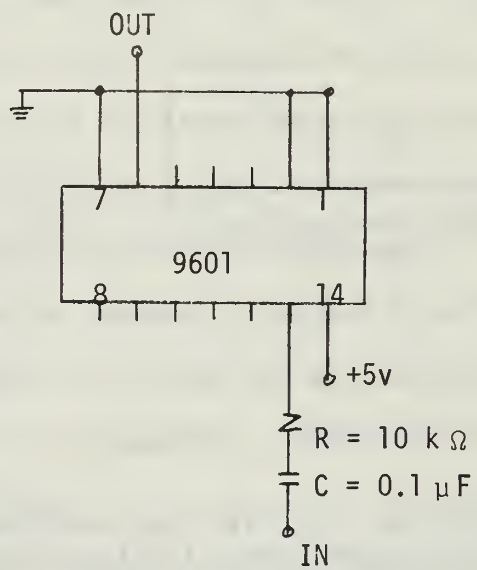


Fig. A-4. CIRCUIT DIAGRAM OF THE BUFFER STAGE

E. DIVIDE-BY-N CIRCUIT

The divide-by-N circuit used is of Sylvania design. The output waveform from this circuit was not suitable for efficient phase comparison. Solutions to this problem are either change the shape of the output waveform or divide by two and compare $f_o/2N$ with 5 kHz in the phase comparator. The latter is used. A CμL9958 decade divider programmed to divide by 2 is used.

F. STABLE REFERENCE SOURCE

The stable reference source consists of a 2 MHz crystal oscillator with a guaranteed frequency accuracy of ±0.0025%, a flip-flop, and three decade dividers. Fig. A-5 is the schematic diagram of the 2 MHz crystal oscillator.

The flip-flop is designed using worst-case design procedures. The circuit is shown in Fig. A-6. In the flip-flop design, we assume an input frequency of 2 MHz, an output frequency of 1 MHz, $I_C = 10$ ma, $V_{CE(SAT)} = 0.3$ v, $V_{BE(SAT)} = 0.75$ v, $H_{FE(min)} = 20$, Q_1 "off", Q_2 "on" and $V_E = 1.5$ V. The following are then calculated:

$$R_e = \frac{1.5}{10 \text{ ma}} = 150\ \Omega \qquad V_{C2} = 1.8\text{V},\ V_{B2} = 2.25\text{V}$$

$$R_B V_{C1} = 2.25 \qquad R_K = R_B\left(\frac{V_{C1}}{2.25} - 1\right)$$

$$V_{C1} = V_{CC} - R_C\left(\frac{2.25}{R_B} + \frac{10 \text{ ma}}{20}\right) = 6 - R_C\left(\frac{2.25}{R_B} + 0.5 \text{ ma}\right)$$

$$V_{C2} = 1.8\text{V} = 6 - R_C\left(10 \text{ ma} + \frac{1.8}{R_B + R_K}\right)$$

$$4.2 = R_C\left(10 \text{ ma} \frac{1.8}{R_B + R_K}\right)$$

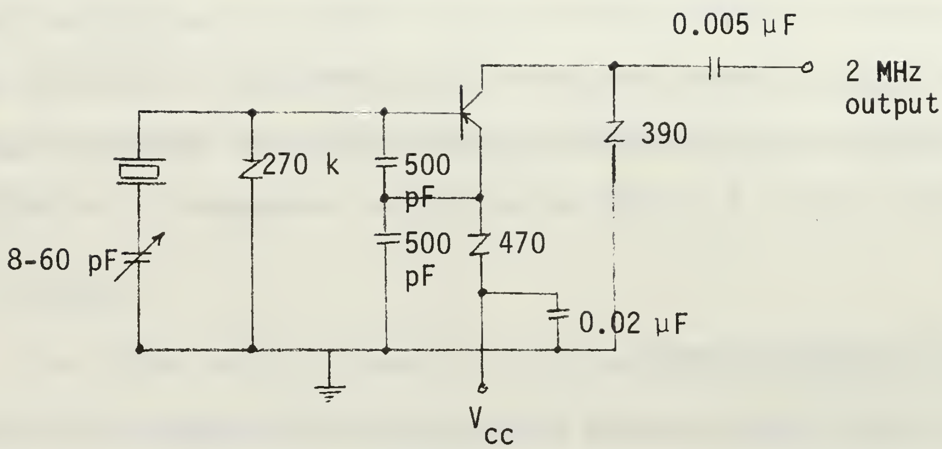


Fig. A-5. CIRCUIT DIAGRAM OF THE 2 MHz CRYSTAL OSCILLATOR

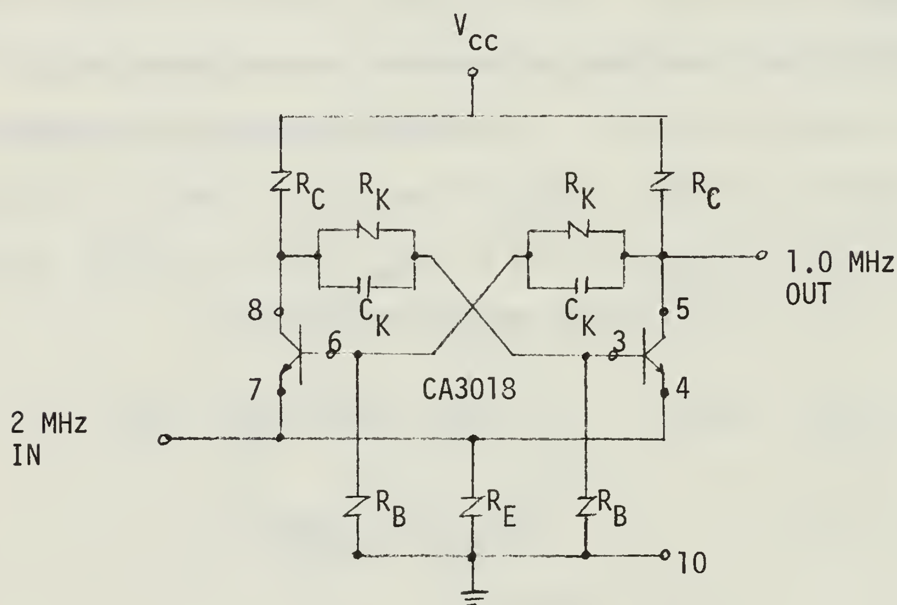


Fig. A-6. CIRCUIT DIAGRAM OF A FLIP-FLOP

We desire $(R_B + R_K)$ large so that the current through the transistor will dominate and determine V_C. Let $R_B = 10$ kΩ, $V_{C1} = 6 - R_C(0.725 \text{ ma})$, and $R_K = 10K\,(2.66 - 0.322\, R_C \text{ ma})$. We desire $V_{C1} = 5.5V$ and $R_C = \frac{0.5}{0.725} = 690\ \Omega$. Let $R_C = 680\ \Omega$. Then $R_K = 24$ kΩ. We require $C_K R \leq \tau$ = period = 1 μsec where $R = R_C + (R_K$ paralleled with $R_B)$. Then $C_K \leq 0.338 \times 10^{-9}$. The optimum value of $C_K = 15$ pF was determined experimentally. Three decade dividers are connected in cascade to divide by 200 to provide output having a frequency of 5 kHz. Fig. A-7 is the complete schematic diagram of the stable reference source.

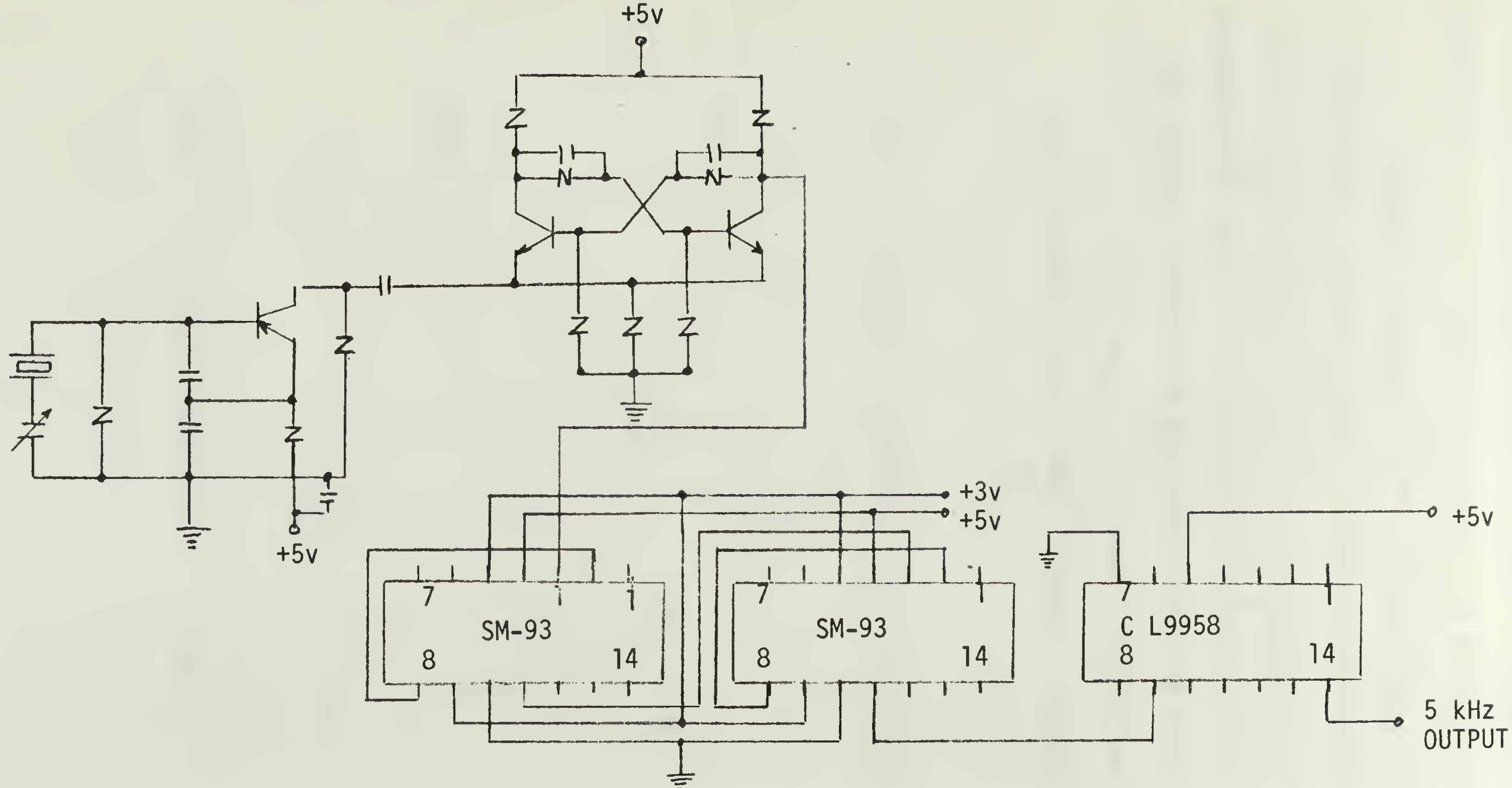


Fig. A-7. CIRCUIT DIAGRAM OF THE 5 kHz STABLE FREQUENCY SOURCE

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13. ABSTRACT

This report presents the results of the design and fabrication of a Multiple-Loop Frequency Synthesizer. The design utilizes frequency control loops to extend the capture range of a phase-locked loop used to provide frequency stability. No harmonic generators, mixers or filters are used, in the usual sense; a single crystal oscillator is required. The synthesizer is small, light weight, accurate to within ± 0.0025% of the programmed frequency, covers the AM broadcast band (500 kHz to 1600 kHz), and is electronically tunable in 10 kHz steps. Unwanted sidebands 5 kHz and 10 kHz away from the programmed frequency have relative magnitudes of -28 db and -40 db, respectively.

14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Frequency Synthesizer						
Phase-Locked-Loop						
Multiple-Loop-Frequency Control						
Voltage-Controlled Oscillators						